USB Keyboard and RGB-LED MCU CH555

Datasheet

Version: 1D

http://wch.cn

1. Overview

The CH555 is USB composite device E8051 core MCU compatible with MCS51 instruction set. 79% of its instructions are single-byte single-cycle instructions, and the average instruction speed is 8 ~ 15 times faster than that of the standard MCS51.

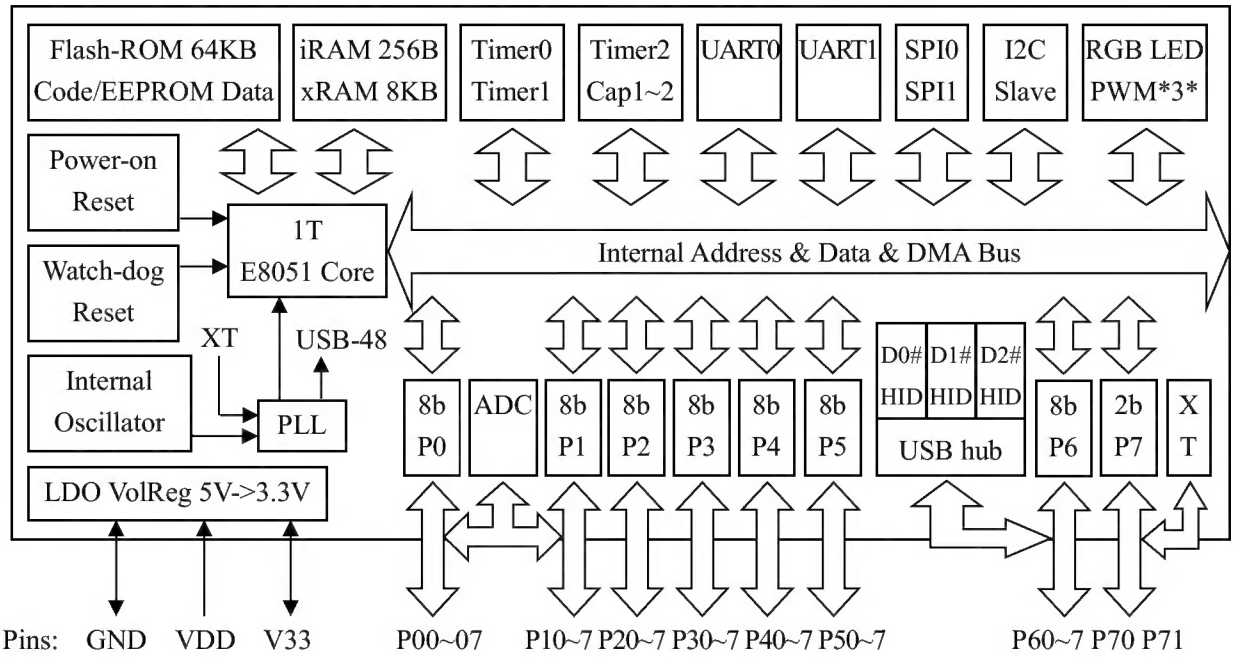
CH555 supports the maximum 32MHz system clock frequency, built-in 64K program memory Flash-ROM and 256-byte internal iRAM and 8 Kbyte of internal xRAM. And xRAM supports direct memory access (DMA).

CH555 has a built-in full-speed composite USB Device controller and receiver-transmitter. The composite USB device controller is composed of a USB device-hub and three HID function sub-devices.

CH555 has built-in three 8-channel PWM, supports either 384 monochrome LEDs or 128 groups of RGB tri-color LEDs.

CH552 is equipped with 12-bit analog-to-digital converter (ADC), built-in clock, 3 timers, 2-channel signal capture, 2 UARTs, SPIs, I2C slave and other function modules.

The following is the internal block diagram of CH555, for reference only.



2. Features

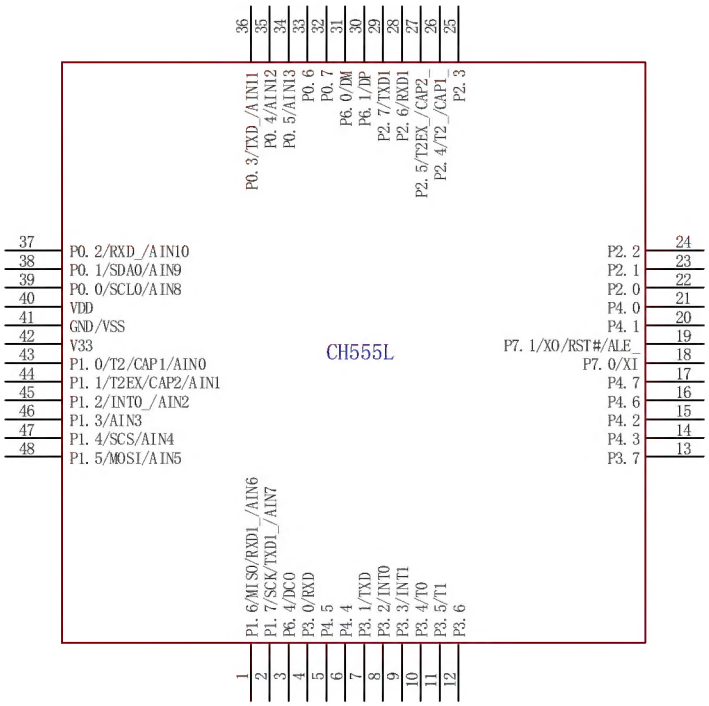
- Core: Enhanced E8051 core, compatible with MCS51 instruction set, 79% of its instructions are single-byte single-cycle instructions, and the average instruction speed is 8 ~ 15 times faster than that of the standard MCS51, with special XRAM data fast copy instruction and double DPTR pointers.

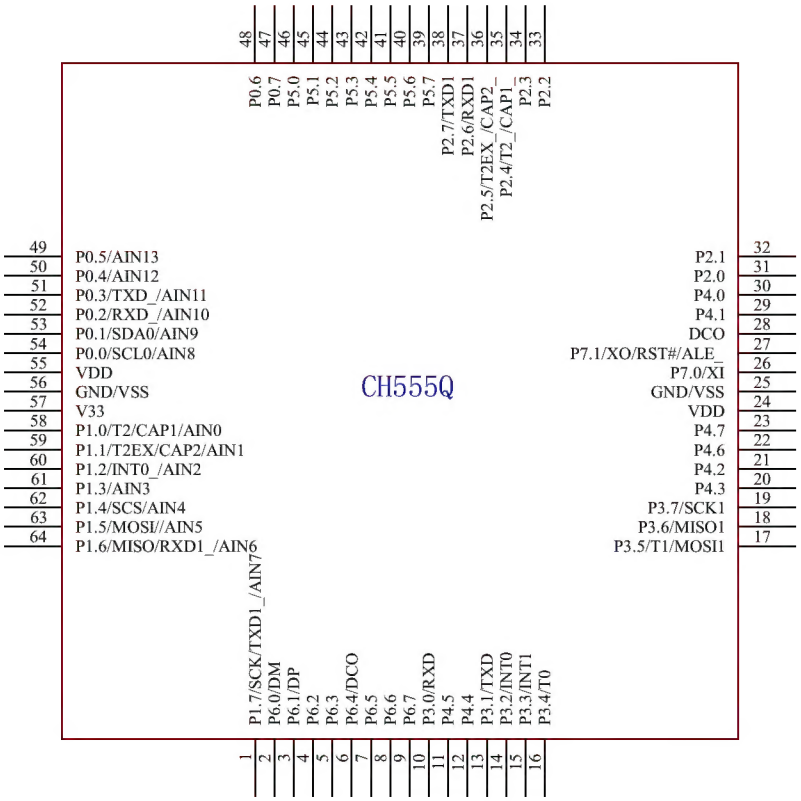
- ROM: Non-volatile memory Flash-ROM with the capacity of 64KB, supports 10K times of erasing/programming, and can all be used for the program address space. Or it can be divided into a 60KB program address space, a 1KB data address space EEPROM and a 3KB BootLoader/ISP program space.
- EEPROM: Data storage area EEPROM has a total of 1K bytes, which is divided into 16 independent blocks, support single-byte read, single-byte write, block write (1 ~ 64 bytes), block erase (64 bytes) operations. In a typical environment, generally it supports 100K times of erasing/programming (non-guaranteed).
- OTP: One Time Programmable data storage area. OTP has a total of 32 bytes, and supports double-word read (4 bytes), single-byte write.
- RAM: 256-byte internal iRAM, can be used for data fast temporary storage and stack. 8KB on-chip xRAM, can be used for large amount of data temporary storage and direct memory access (DMA).
- USB: It has a built-in USB composite device controller and USB receiver-transmitter, composed of a USB device-hub and three HID function sub-devices, totally 24 USB endpoints. Support USB 2.0 full-speed (12Mbps) traffic, built-in FIFO, support 64-byte data packet and DMA.
- Timer: 3 sets of 16-bit timers (T0, T1 and T2), which are standard MCS51 timers.
- Capture: Timer T2 is extended to support 2-channel signal capture, support leading edge trigger, lagging edge trigger, periodic detection.
- UART: 2 UARTs. UART0 is a standard MCS51 serial port, UART1 has built-in communication baud rate setting register.
- SPI: 2 channels of SPIs, with built-in FIFO, the clock frequency can be approximate to half of the system clock frequency Fsys. Support simplex multiplexing of serial data input and output. SPI0 controller supports Master/Slave mode, while SPI1 controller only supports Master mode.
- I2CS: I2C slave controller, support DMA, used for EEPROM memory 24C.
- RGB LED: Support 384 monochrome LEDs or 128 sets of RGB tri-color LEDs through 3*8 channels of PWM and 1/16 dynamic scanning. The maximum 8-bit brightness PWM supports 256-level of grayscale and the maximum 3*8-bit color PWM supports 16777216 sets of combined colors. The dedicated DMA mode supports load preset curing data from Flash-ROM or load edited data from xRAM.
- ADC: 14-channel 12-bit A/D converter.
- GPIO: The chip in LQFP48 package supports up to 45 GPIO pins and the chip in LQFP64 package supports up to 58 GPIO pins (including XI and USB pins), support MCS51 compatible quasi-bidirectional mode, newly add high-impedance input, push-pull output, open-drain output mode.
- Interrupt: Support 14 sets of interrupt signal sources, including 6 sets of interrupts compatible with the standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and 8 sets of extended interrupts (SPI0, USB, ADC, UART1, LED/I2C, GPIO, WDOG). Among them, GPIO interrupt can be selected from multiple pins.
- Watch-Dog: 8-bit presettable watchdog timer WDOG, support timing interrupt.
- Reset: 5 types of reset signal sources. Built-in power on reset and multi-stage adjustable power low voltage detection reset module, software reset and watchdog overflow reset, optional pin for external input reset.
- Clock: Built-in 24MHz clock source, can support external crystals by multiplexing GPIO pins, and the built-in PLL is used to generate the USB clock and the system clock frequency Fsys with the required frequency.
- Power: Built-in 5V to 3.3V low dropout voltage regulator for USB and other modules. It supports 5V

or 3.3V or even 6V or 2.8V power supply. Built-in DC-DC controller, can control the external MOS tube to achieve voltage boost.

- Sleep: Support low-power sleep mode, support externally wake up USB, UART0, UART1, SPI0, and part of the GPIOs.
- Built-in unique ID, support ID number and calibration.

3. Package





Package	Body size		Lead pitch		Description	Part No.
LQFP-48	7*7mm		0.5mm	19.7mil	Standard LQFP 48-pin patch	CH555L
LQFP-64	7*7mm		0.4mm	15.7mil	Standard LQFP 64-pin patch	CH555Q

4. Pin definitions

Pin No.		Pin Name	Alternate (Left function with the highest priority)	Description
CH555Q	CH555L			
55, 24	40	VDD	VCC	I/O power input and external power input of internal USB power regulator, require an external 0.1uF power decoupling capacitor.
57	42	V33	V3	Internal USB power regulator output and internal USB power input, When supply voltage is less than 3.6V, connect VDD to input the external power. When supply voltage is greater than 3.6V, connect an external 0.1uF power decoupling capacitor.
56, 25	41	GND	VSS	Common ground.
54	39	P0.0	SCL0/AIN8	AIN8 ~ AIN13: 6-channel ADC analog signal/touch key input. RXD_, TXD_: RXD, TXD pin mapping. SCL0, SDA0: I2CS serial clock input, bidirectional serial data. Level change on any pin from P0.0 to P0.7 supports interrupt and wake up.
53	38	P0.1	SDA0/AIN9	
52	37	P0.2	RXD_/AIN10	
51	36	P0.3	TXD_/AIN11	
50	35	P0.4	AIN12	
49	34	P0.5	AIN13	
48	33	P0.6		
47	32	P0.7		
58	43	P1.0	T2/CAP1/AIN0	AIN0 ~ AIN7: 8-channel ADC analog signal/touch key input. T2: External count input/clock output of timer/counter 2. T2EX: Reload/capture input of timer/counter 2. CAP1, CAP2: Capture input 1, 2 of timer/counter 2. SCS, MOSI, MISO, SCK: SPI0 interface, SCS is chip selection input, MOSI is host output/slave input, MISO is host input/slave output, SCK is serial clock host output/slave input. INT0_, RXD1_, TXD1_: INT0/RXD1/TXD1 pin mapping. Level change on any pin from P1.0 to P1.3 supports interrupt and wake up.
59	44	P1.1	T2EX/CAP2/AIN1	
60	45	P1.2	INT0_/AIN2	
61	46	P1.3	AIN3	
62	47	P1.4	SCS/AIN4	
63	48	P1.5	MOSI/AIN5	
64	1	P1.6	MISO/RXD1_/AIN6	
1	2	P1.7	SCK/TXD1_/AIN7	
31	22	P2.0		T2_/CAP1_: T2/CAP1 pin mapping. T2EX_/CAP2_: T2EX/CAP2 pin mapping. RXD1, TXD1: serial data input, serial data output of
32	23	P2.1		
33	24	P2.2		

34	25	P2.3		UART1. Level change on any pin from P2.0 to P2.3 supports interrupt and wake up.
35	26	P2.4	T2_/CAP1_	
36	27	P2.5	T2EX_/CAP2_	
37	28	P2.6	RXD1	
38	29	P2.7	TXD1	
10	4	P3.0	RXD	RXD, TXD: serial data input, serial data output of UART0. INT0, INT1: external interrupt 0, external interrupt 1 input. T0, T1: timer 0, timer 1 external input. MOSI1, MISO1, SCK1: SPI1 interface, host output. MISO is host input. SCK is serial clock output.
13	7	P3.1	TXD	
14	8	P3.2	INT0	
15	9	P3.3	INT1	
16	10	P3.4	T0	
17	11	P3.5	MOSI1/T1	
18	12	P3.6	MISO1	
19	13	P3.7	SCK1	
30	21	P4.0		Level change on any pin from P4.0 to P4.7 supports interrupt and wake up. If P4_LED_KEY corresponds to bit 1, it has the following characteristics: Support current keyboard signal input when pin is input or bidirectional. When pin is output, no series current limiting resistor is needed, drive LED directly.
29	20	P4.1		
21	15	P4.2		
20	14	P4.3		
12	6	P4.4		
11	5	P4.5		
22	16	P4.6		
23	17	P4.7		
46	None	P5.0		I/O supply of P5.0 ~ P5.7 is V33, input voltage does not exceed V33.
45	None	P5.1		
44	None	P5.2		
43	None	P5.3		
42	None	P5.4		
41	None	P5.5		
40	None	P5.6		
39	None	P5.7		
2	31	P6.0	DM	DM, DP: D- and D+ signal of USB composite device. The transceiver is designed built-in based on USB2.0. and the pins are not connected to resistors in series. DCO: DC-DC drive output. I/O supply of P6.0 ~ P6.7 is V33, input voltage does not exceed V33. And separate controllable 7.5K pull-up resistors to VDD are provided by P6.0 ~ P6.7.
3	30	P6.1	DP	
4	None	P6.2		
5	None	P6.3		
6	3	P6.4	DCO	
7	None	P6.5		
8	None	P6.6		
9	None	P6.7		
26	18	P7.0	XI	XI, XO: input and inverted output of external crystal oscillator. ALE_: ALE pin mapping. RST#: External reset input, active at low level, built-in pull-up resistor.
27	19	P7.1	XO/RST#/ALE_	
28	None	DCO		DC-DC drive output

After RGB LED of CH555 is enabled, some pins are optionally alternate for PWM driver or dynamic scanning driver.

Pin Name	Function Name	Function Description
P4.0～P4.7	RED0～RED7	RGB LED red PWM drive output, each bit can be independently enabled and disabled.
P2.0～P2.7	GRE0～GRE7	RGB LED green PWM drive output, each bit can be independently enabled and disabled.
P1.0～P1.7	BLU0～BLU7	RGB LED blue PWM drive output, each bit can be independently enabled and disabled.
P7.0～P7.1	COM14～COM15	RGB LED dynamic scanning public drive output, each bit can be independently enabled and disabled.
P0.0～P0.7	COM16～COM23	RGB LED dynamic scanning public drive output, each bit can be independently enabled and disabled.
P3.0～P3.7	COM24～COM31	RGB LED dynamic scanning public drive output, each bit can be independently enabled and disabled.

5. Special function register (SFR)

The following abbreviations may be used in this datasheet to describe the registers:

Abbreviation	Description
RO	Software can only read these bits.
WO	Software can only write to this bit. The read value is invalid.
RW	Software can read and write to these bits.
H	End with it to indicate a hexadecimal number
B	End with it to indicate a binary number

5.1 Introduction to SFR and address distribution

CH555 controls and manages the device, and sets the working mode via special function registers (SFR and xSFR).

SFR occupies 80h-FFh address range of the internal data storage space and can only be accessed by direct address commands. The registers with the x0h address and the x8h address are addressed in bits to avoid modifying the values of other bits when accessing a specific bit. Other registers with addresses that are not the multiple of 8 can only be accessed by bytes.

Some SFRs can only be written in safe mode, while they can be read only in non-safe mode , for example: GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL, POWER_CFG, GPIO_IE.

Some SFRs have one or more aliases, for example: SPI0_CK_SE/SPI0_S_PRE, ROM_ADDR_L/ROM_DATA_LL, ROM_ADDR_H/ROM_DATA_LH, ROM_DATA_HL/ROM_DAT_BUF, ROM_DATA_HH/ROM_BUF_MOD.

Some addresses correspond to multiple independent SFRs, for example: SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

CH555 contains all 8051 standard SFR registers. In addition, other device control registers are added. See the table below for SFRs.

Table 5.1.1 Internal special function registers (SFR)

SFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP	A_INV	RESET_KEEP	WDOG_COUNT
0xF0	B	P7_IO		ADC_CTRL	ADC_DAT_L	ADC_DAT_H	ADC_CHAN	LED_STATUS
0xE8	IE_EX	IP_EX						
0xE0	ACC							
0xD8								
0xD0	PSW							
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	P4	P4_LED_KEY	P4_MOD_OC	P4_DIR_PU	P0_MOD_OC	P0_DIR_PU	LED_DMA_L	LED_DMA_H
0xB8	IP	CLOCK_CFG	POWER_CFG	I2CS_INT_ST	SCON1	SBUF1	SBAUD1	SIF1
0xB0	P3	GLOBAL_CFG	GPIO_IE	I2CX_INT	SPI1_STAT	SPI1_DATA	SPI1_CTRL	SPI1_CK_SE
0xA8	IE	WAKE_CTRL	P5_IN	P5_OUT_PU	P5_OE	P6_IN	P6_OUT_PU	P6_OE
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX				LED_COMMON	LED_PIN_OE
0x98	SCON	SBUF						
0x90	P1		P1_MOD_OC	P1_DIR_PU	P2_MOD_OC	P2_DIR_PU	P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_HL ROM_DAT_BUF	ROM_DATA_HH ROM_BUF_MOD
0x80	P0	SP	DPL	DPH	ROM_ADDR_L ROM_DATA_LL	ROM_ADDR_H ROM_DATA_LH	ROM_CTRL ROM_STATUS	PCON

Notes : (1) Those in red text can be addressed in bits;

(2). The following table shows the description of the color box

	Register address
	SPI0 related register
	SPI1 related register
	ADC related register
	Timer/counter2 related register
	Port setting related register
	UART1 related register
	Timer/counter0 and 1 related register
	I2C related register
	RGB LED PWM related register
	Flash-ROM related register
	USB related register

xSFR occupies the 2000H-3FFFH address range of the external data storage space and actually uses only part of addresses within the range of 2100H-22FFH. After bXIR_XSFR is set to 1, MOVX_@R0/R1 command will be dedicated to accessing xSFR, and some xSFRs will be able to imitate the pdata feature of the external data storage space for quick access by aliasing the original name with a P character. For example, in C program language, read/write I2CS_CTRL by accessing the xSFR with xdata feature in the address range of 2100H-22FFH through DPTR long pointer. Read/write pI2CS_CTRL by accessing the xSFR with pdata feature in the address range of 00H-FFH through R0 or R1 short pointer.

Some addresses correspond to multiple independent SFRs, for example: Dn_EP6T_L/Dn_RX_LEN, n is 0/1/2.

Table 5.1.2 External special function registers (xSFR) with pdata feature

xSFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
Other								
0xE8	ANA_PIN	PIN_FUNC	PORT_CFG	CMP_DCDC				
0xD8	LED_INT_ADJ	LED_RED_ADJ	LED_GRE_ADJ	LED_BLU_ADJ	LED_FRA_STA	LED_COL_CNT		
0xD0		LED_CTRL	LED_CYCLE	LED_FRAME				
0x38	HB_EP0T_L	HB_EP1T_L	I2CS_STAT	USB_IE	USB_CTRL	USB_IF	HB_RX_LEN	HB_STATUS
0x30	HB_EP0RES	HB_EP1RES	I2CS_CTRL	I2CS_DEV_A	HB_EP4RES	I2CS_ADDR	I2CS_DATA	HB_ADDR
0x28	D2_EP0T_L	D2_EP1T_L	D2_EP2T_L	D2_EP3T_L	D2_EP_MOD	D2_EP5T_L	D2_EP6T_L D2_RX_LEN	D2_STATUS
0x20	D2_EP0RES	D2_EP1RES	D2_EP2RES	D2_EP3RES	D2_EP4RES	D2_EP5RES	D2_EP6RES	D2_ADDR
0x18	D1_EP0T_L	D1_EP1T_L	D1_EP2T_L	D1_EP3T_L	D1_EP_MOD	D1_EP5T_L	D1_EP6T_L D1_RX_LEN	D1_STATUS
0x10	D1_EP0RES	D1_EP1RES	D1_EP2RES	D1_EP3RES	D1_EP4RES	D1_EP5RES	D1_EP6RES	D1_ADDR
0x08	D0_EP0T_L	D0_EP1T_L	D0_EP2T_L	D0_EP3T_L	D0_EP_MOD	D0_EP5T_L	D0_EP6T_L D0_RX_LEN	D0_STATUS
0x00	D0_EP0RES	D0_EP1RES	D0_EP2RES	D0_EP3RES	D0_EP4RES	D0_EP5RES	D0_EP6RES	D0_ADDR

5.2 SFR/xSFR classification and reset value

Figure 5.2 SFR and xSFR description and reset value

Function Classification	Name	Address	Description	Reset value
System setting related Register	B	F0h	B register	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	A_INV	FDh	Inversion value of high and low bits of accumulator	0000 0000b
	PSW	D0h	Program status word register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (in boot loader state)	0010 0000b
			Global configuration register (in application program state)	0000 0000b
	CHIP_ID	A1h	ID code of chip (read-only)	0101 0110b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b
	DPH	83h	The higher 8 bits of data address pointer	0000 0000b
	DPL	82h	The lower 8 bits of data address pointer	0000 0000b
	DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power control related register	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Reset keep register (in power on reset state)	0000 0000b
	POWER_CFG	BAh	Power management configuration register	0000 0xxxb
	CLOCK_CFG	B9h	System clock configuration register	1000 0011b
	WAKE_CTRL	A9h	Sleep wake-up control register	0000 0000b

	PCON	87h	Power supply control register (in power on reset state)	0001 0000b
	CMP_DCDC	21EBh	Comparator and DC-DC control register	0000 0000b
Interrupt control related registers	IP_EX	E9h	Extend interrupt priority control register	0000 0000b
	IE_EX	E8h	Extend interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
	GPIO_IE	B2h	GPIO interrupt enable register	0000 0000b
Flash-ROM related registers	ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HI	8Eh	ROM_DATA_HL and ROM_DATA_HH constitute a 16-bit SFR	xxxxh
	ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_STATUS	86h	flash-ROM status register (read only)	0000 0000b
	ROM_CTRL	86h	flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h	flash-ROM address register high byte	xxxx xxxxb
	ROM_ADDR_L	84h	flash-ROM address register low byte	xxxx xxxxb
	ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh
	ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LO	84h	ROM_DATA_LL and ROM_DATA_LH constitute a 16-bit SFR	xxxxh
Port setting related register	XBUS_AUX	A2h	External bus auxiliary setting register	0000 0000b
	P7	F1h	P7 port input and output register	00PP 0011b
	P0_DIR_PU	C5h	P0 port direction control and pull-up enable register	1111 1111b
	P0_MOD_OC	C4h	P0 port output mode register	1111 1111b
	P4_DIR_PU	C3h	P4 port direction control and pull-up enable register	1111 1111b
	P4_MOD_OC	C2h	P4 port output mode register	1111 1111b
	P4_LED_KEY	C1h	P4 port LED current limit and keyboard mode register	0000 0000b
	P6_DIR	AFh	P6 port direction control register	0000 0000b
	P6_OUT_PU	AEh	P6 port output data and pull-up enable register	0000 0000b
	P6_IN	ADh	P6 port input register	PPPP PPPPb

	P5_DIR	ACh	P5 port direction control register	0000 0000b
	P5_OUT_PU	ABh	P5 port output data and pull-up enable register	0000 0000b
	P5_IN	AAh	P5 port input register	PPPP PPPPb
	P3_DIR_PU	97h	P3 port direction control and pull-up enable register	1111 1111b
	P3_MOD_OC	96h	P3 port output mode register	1111 1111b
	P2_DIR_PU	95h	P2 port direction control and pull-up enable register	1111 1111b
	P2_MOD_OC	94h	P2 port output mode register	1111 1111b
	P1_DIR_PU	93h	P1 port direction control and pull-up enable register	1111 1111b
	P1_MOD_OC	92h	P1 port output mode register	1111 1111b
	P4	C0h	P4 port input and output register	1111 1111b
	P3	B0h	P3 port input and output register	1111 1111b
	P2	A0h	P2 port input and output register	1111 1111b
	P1	90h	P1 port input and output register	1111 1111b
	P0	80h	P0 port input and output register	1111 1111b
	PORT_CFG	21EAh	Port interrupt and wake-up configuration register	0000 0000b
	PIN_FUNC	21E9h	Pin function selection register	0000 0000b
	ANA_PIN	21E8h	Analog pin digital input disable register	0000 0000b
Timer/counter 0 and 1 related registers	TH1	8Dh	Timer1 counter high byte	xxxx xxxxb
	TH0	8Ch	Timer0 counter high byte	xxxx xxxxb
	TL1	8Bh	Timer1 counter low byte	xxxx xxxxb
	TL0	8Ah	Timer0 counter low byte	xxxx xxxxb
	TMOD	89h	Timer0/1 mode register	0000 0000b
	TCON	88h	Timer0/1 control register	0000 0000b
UART0 related registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timer/Counter 2 related registers	T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxxx xxxxb
	T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxxx xxxxb
	T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	xxxxh
	TH2	CDh	Timer2 counter high byte	0000 0000b
	TL2	CCh	Timer2 counter low byte	0000 0000b
	T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
	RCAP2H	CBh	Count reload/capature 2 data register high byte	0000 0000b
	RCAP2L	CAh	Count reload/capature 2 data register low byte	0000 0000b
	RCAP2	CAh	RCAP2L and RCAP2H constitute a 16-bit SFR	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b

	T2CON	C8h	Timer2 control register	0000 0000b
SPI0 related registers	SPI0_SETUP	FCh	SPI0 setting register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock frequency division setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data receiving/transmitting register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 status register	0000 1000b
UART1 related registers	SIF1	BFh	UART1 interrupt status register	0000 0000b
	SBAUD1	BEh	UART1 baud rate setting register	xxxx xxxxb
	SBUF1	BDh	UART1 data register	xxxx xxxxb
	SCON1	BCh	UART1 control register	0000 0000b
SPI1 related registers	SPI1_CK_SE	B7h	SPI1 clock frequency division setting register	0010 0000b
	SPI1_CTRL	B6h	SPI1 control register	0000 0010b
	SPI1_DATA	B5h	SPI1 data receive/transmit register	xxxx xxxxb
	SPI1_STAT	B4h	SPI1 status register	0000 1000b
ADC related registers	ADC_CHAN	F6h	ADC analog signal channel selection register	0000 0000b
	ADC_DAT_H	F5h	ADC result data high byte (read only)	0000 xxxxb
	ADC_DAT_L	F4h	ADC result data low byte (read only)	xxxx xxxxb
	ADC_DAT	F4h	ADC_DAT_L and ADC_DAT_H constitute a 16-bit SFR	0xxxh
	ADC_CTRL	F3h	ADC control and status register	x000 000xb
I2C Slave related registers	I2CS_INT_ST	BBh	Mapping of I2CS slave status register I2CS_STAT	0000 1100b
	I2CX_INT	B3h	I2C and RGB LED interrupt request register	0000 0000b
	I2CS_STAT	223Ah	I2CS slave status register	0000 1100b
	I2CS_DATA	2236h	I2CS slave data receive/transmit register	xxxx xxxxb
	I2CS_ADDR	2235h	I2CS slave data address register (read-only)	xxxx xxxxb
	I2CS_DEV_A	2233h	I2CS slave device address register	0000 0000b
	I2CS_CTRL	2232h	I2CS slave control register	0000 0x00b
	I2CS_DMA_L	2139h	I2CS slave buffer start address low byte	xxxx xxxxb
	I2CS_DMA_H	2138h	I2CS slave buffer start address highr byte	000x xxxxb
USB function subdevice D0 related registers	D0_EP0RES	2200h	USBD0 endpoint0 control register	0000 0000b
	D0_EP1RES	2201h	USBD0 endpoint1 control register	0000 0000b
	D0_EP2RES	2202h	USBD0 endpoint2 control register	0000 0000b
	D0_EP3RES	2203h	USBD0 endpoint3 control register	0000 0000b
	D0_EP4RES	2204h	USBD0 endpoint4 control register	0000 0000b
	D0_EP5RES	2205h	USBD0 endpoint5 control register	0000 0000b
	D0_EP6RES	2206h	USBD0 endpoint6 control register	0000 0000b
	D0_ADDR	2207h	USBD0 device address register	0000 0000b
	D0_EP0T_L	2208h	USBD0 endpoint0 transmission length	0xxx xxxxb

			register	
	D0_EP1T_L	2209h	USBD0 endpoint1 transmission length register	0xxx xxxxb
	D0_EP2T_L	220Ah	USBD0 endpoint2 transmission length register	0xxx xxxxb
	D0_EP3T_L	220Bh	USBD0 endpoint3 transmission length register	0xxx xxxxb
	D0_EP_MOD	220Ch	USBD0 endpoint mode control register	0000 0000b
	D0_EP5T_L	220Dh	USBD0 endpoint5 transmission length register	00xx xxxxb
	D0_EP6T_L	220Eh	USBD0 endpoint6 transmission length register	00xx xxxxb
	D0_RX_LEN	220Eh	USBD0 reception length register (read-only)	0xxx xxxxb
	D0_STATUS	220Fh	USBD0 status register	0001 1xxxb
USB function subdevice D1 related registers	D1_EP0RES	2210h	USBD1 endpoint0 control register	0000 0000b
	D1_EP1RES	2211h	USBD1 endpoint1 control register	0000 0000b
	D1_EP2RES	2212h	USBD1 endpoint2 control register	0000 0000b
	D1_EP3RES	2213h	USBD1 endpoint3 control register	0000 0000b
	D1_EP4RES	2214h	USBD1 endpoint4 control register	0000 0000b
	D1_EP5RES	2215h	USBD1 endpoint5 control register	0000 0000b
	D1_EP6RES	2216h	USBD1 endpoint6 control register	0000 0000b
	D1_ADDR	2217h	USBD1 device address register	0000 0000b
	D1_EP0T_L	2218h	USBD1 endpoint0 transmission length register	0xxx xxxxb
	D1_EP1T_L	2219h	USBD1 endpoint1 transmission length register	0xxx xxxxb
	D1_EP2T_L	221Ah	USBD1 endpoint2 transmission length register	0xxx xxxxb
	D1_EP3T_L	221Bh	USBD1 endpoint3 transmission length register	0xxx xxxxb
	D1_EP_MOD	221Ch	USBD1 endpoint mode control register	0000 0000b
	D1_EP5T_L	221Dh	USBD1 endpoint5 transmission length register	00xx xxxxb
	D1_EP6T_L	221Eh	USBD1 endpoint6 transmission length register	00xx xxxxb
	D1_RX_LEN	221Eh	USBD1 reception length register (read-only)	0xxx xxxxb
	D1_STATUS	221Fh	USBD1 status register	0001 1xxxb
USB function subdevice D2 related registers	D2_EP0RES	2220h	USBD2 endpoint0 control register	0000 0000b
	D2_EP1RES	2221h	USBD2 endpoint1 control register	0000 0000b
	D2_EP2RES	2222h	USBD2 endpoint2 control register	0000 0000b
	D2_EP3RES	2223h	USBD2 endpoint3 control register	0000 0000b
	D2_EP4RES	2224h	USBD2 endpoint4 control register	0000 0000b
	D2_EP5RES	2225h	USBD2 endpoint5 control register	0000 0000b
	D2_EP6RES	2226h	USBD2 endpoint6 control register	0000 0000b

	D2_ADDR	2227h	USBD2 device address register	0000 0000b
	D2_EP0T_L	2228h	USBD2 endpoint0 transmission length register	0xxx xxxxb
	D2_EP1T_L	2229h	USBD2 endpoint1 transmission length register	0xxx xxxxb
	D2_EP2T_L	222Ah	USBD2 endpoint2 transmission length register	0xxx xxxxb
	D2_EP3T_L	222Bh	USBD2 endpoint3 transmission length register	0xxx xxxxb
	D2_EP_MOD	222Ch	USBD2 endpoint mode control register	0000 0000b
	D2_EP5T_L	222Dh	USBD2 endpoint5 transmission length register	00xx xxxxb
	D2_EP6T_L	222Eh	USBD2 endpoint6 transmission length register	00xx xxxxb
	D2_RX_LEN	222Eh	USBD2 reception length register (read-only)	0xxx xxxxb
	D2_STATUS	222Fh	USBD2 status register	0001 1xxxb
USB global and hub related registers	HB_EP0RES	2230h	USBHB endpoint0 control register	0000 0000b
	HB_EP1RES	2231h	USBHB endpoint1 control register	0000 0000b
	HB_EP4RES	2234h	USBHB endpoint4 control register	0000 0000b
	HB_ADDR	2237h	USBHB device address register	0000 0000b
	HB_EP0T_L	2238h	USBHB endpoint0 transmission length register	0xxx xxxxb
	HB_EP1T_L	2239h	USBHB endpoint1 transmission length register	00xx xxxxb
	USB_IE	223Bh	USB interrupt enable register	0010 0000b
	USB_CTRL	223Ch	USB control register	0000 011xb
	USB_IF	223Dh	USB interrupt flag register	0000 x000b
	HB_RX_LEN	223Eh	USBHB reception length register (read-only)	0xxx xxxxb
	HB_STATUS	223Fh	USBHB status register	0001 1xxxb
RGB LED related registers	LED_STATUS	F7h	RGB LED status register	0001 xxxxb
	LED_DMA_H	C7h	RGB LED buffer area current address high byte	xxxx xxxxb
	LED_DMA_L	C6h	RGB LED buffer area current address low byte	xxxx xxxxb
	LED_DMA	C6h	LED_DMA_L and LED_DMA_H constitute a 16-bit SFR	xxxxh
	LED_PWM_OE	A7h	RGB LED drive PWM pin enable register	0000 0000b
	LED_COMMON	A6h	RGB LED drive COMMON pin selection register	0000 0000b
	LED_COL_CNT	21DDh	RGB LED color counter register (read only)	0000 0000b
	LED_FRA_STA	21DCh	RGB LED frame status register (read only)	0000 0000b
	LED_BLU_ADJ	21DBh	RGB LED blue adjustment register	0000 0000b
	LED_GRE_ADJ	21DAh	RGB LED green adjustment register	0000 0000b

	LED_RED_ADJ	21D9h	RGB LED red adjustment register	0000 0000b
	LED_INT_ADJ	21D8h	RGB LED brightness adjustment register	0000 0000b
	LED_FRAME	21D3h	RGB LED frame configuration register	0000 0000b
	LED_CYCLE	21D2h	RGB LED cycle configuration register	0000 0000b
	LED_CTRL	21D1h	RGB LED control register	0000 0000b

5.3 General-purpose 8051 registers

Table 5.3.1 General-purpose 8051 registers

Name	Address	Description	Reset value
A_INV	FDh	Inverted value of high and low bits of accumulator	00h
B	F0h	B register	00h
A, ACC	E0h	Accumulator	00h
PSW	D0h	Program status word register	00h
GLOBAL_CFG	B1h	Global configuration register (in boot loader state)	20h
		Global configuration register (in application program state)	00h
CHIP_ID	A1h	ID code of chip (read-only)	56h
SAFE_MOD	A1h	Safe mode control register (write only)	00h
PCON	87h	Power supply control register (in power on reset state)	10h
DPH	83h	The higher 8 bits of data address pointer	00h
DPL	82h	The lower 8 bits of data address pointer	00h
DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
SP	81h	Stack pointer	07h

B register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic operation register, mainly used for multiplication and division operations, addressed in bits	00h

A accumulator (A, ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic operation accumulator, addressed in bits	00h

Program status word register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry flag bit: used to record the carry or borrow of the highest bit when performing arithmetic operations and logical operations. In 8-bit addition operation, for the carry of the highest bit, the bit will be set, otherwise it will be cleared. In 8-bit subtraction operation, for the borrow, the bit will be set, otherwise it will be cleared. The logical command can set or clear the bit	0
6	AC	RW	Auxiliary carry flag bit: in addition and subtraction operations, carry or borrow from the higher 4 bits to the	0

			lower 4 bits, AC will be set, otherwise it will be cleared.	
5	F0	RW	Common flag bit 0 addressed in bits: user-defined, can be cleared or set by software	0
4	RS1	RW	High bit of register bank selection bit	0
3	RS0	RW	Low bit of register bank selection bit	0
2	OV	RW	Overflow flag bit: in addition and subtraction operations, if the operation result exceeds 8-bit binary number, OV will be set as 1 and the flag will overflow, otherwise it will be cleared to 0.	0
1	F1	RW	Common flag bit 1 addressed in bits: user-defined, can be cleared or set by software	0
0	P	RO	Parity flag bit: record the parity of 1 in accumulator A after the command is executed. If the number of '1' is an odd number, P will be set. If the number of '1' is an even number, P will be cleared.	0

The state of processor is stored in the PSW register, and PSW can be addressed in bits. The status word includes the carry flag bit, auxiliary carry flag bit for BCD code processing, parity flag bit, overflow flag bit, as well as RS0 and RS1 for working register bank selection.The area where the working register bank is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 working register bank selection

RS1	RS0	Working register bank
0	0	Bank 0 (00h-07h)
0	1	Bank 1 (08h-0Fh)
1	0	Bank 2 (10h-17h)
1	1	Bank 3 (18h-1Fh)

Table 5.3.3 Operations that affect flag bits (X refers that flag bit is related to the operation result)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data address pointer (DPTR):

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH constitute a16-bit data pointer DPTR, used to access xSFR, xBUS, xRAM data memory or program memory. The actual DPTR corresponds to two sets of physical 16-bit data pointers, DPTR0 and DPTR1, dynamically selected by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer, mainly used for program calls and interrupt calls as well as data in and out of stack	07h

Specific function of stack: protect breakpoint and protect site, and carry out management on the first-in last-out principle. During instack, SP pointer will automatically add 1, save the data or breakpoint information. During outstack, SP pointer will point to the data unit and automatically substract 1. The initial value of SP is 07h after reset, and the corresponding default stack storage starts from 08h.

5.4 Special registers

Inverted value of high and low bits of accumulator (A_INV):

Bit	Name	Access	Description	Reset value
[7:0]	A_INV	RO	Inverted value of high and low bits of accumulator, result of bit 0 ~ bit 7 according to a reverse bit order, Bit 7 and bit 6 ~ bit 0 of A_INV are bit 0 and bit 1 ~ bit 7 of ACC respectively	00h

Global configuration register (GLOBAL_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Reserved	00b
5	bBOOT_LOAD	RO	Boot loader status bit, used to distinguish ISP boot loader state or application state: set 1 during power on, cleared to 0 during software reset. For the chip with ISP boot loader, if the bit is 1, it indicates that it has never been reset by software and it is usually in running state of ISP boot loader after power on. If the bit is 0, it indicates that it has been reset by software, and usually in application state.	1
4	bSW_RESET	RW	Software reset control bit: setting 1 will cause software reset. Automatically cleared by hardware	0
3	bCODE_WE	RW	Flash-ROM write enable bit: 0: Write protection; 1: Flash-ROM can be written and erased.	0
2	bDATA_WE	RW	DataFlash area of Flash-ROM write enable bit: 0: Write protection; 1: DataFlash area can be written and erased.	0
1	bXIR_XSFR	RW	MOVX_@R0/R1 command access range control bit: 0: It allows access all xRAM/xSFR in xdata area; 1: It is dedicated to access xSFR rather than xRAM.	0
0	bWDOG_EN	RW	Watchdog reset enable bit:	0

			0: Watchdog is only used as timer; 1: Watchdog reset is allowed to be generated during timing overflow.	

Safe mode control register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	Used to enter or terminate safe mode	00h

Some SFRs can only be written in safe mode, while they are always read-only in non-safe mode. Steps to enter safe mode are as follows:

(1). Write 55h into this register;

(2). And then write AAh into this register;

(3). After that, it is in safe mode for about 13 to 23 system clock frequency cycles, and one or more safe class SFR or ordinary SFR can be rewritten in such validity period.

(4). Automatically terminate the safe mode after the expiration of the above validity period

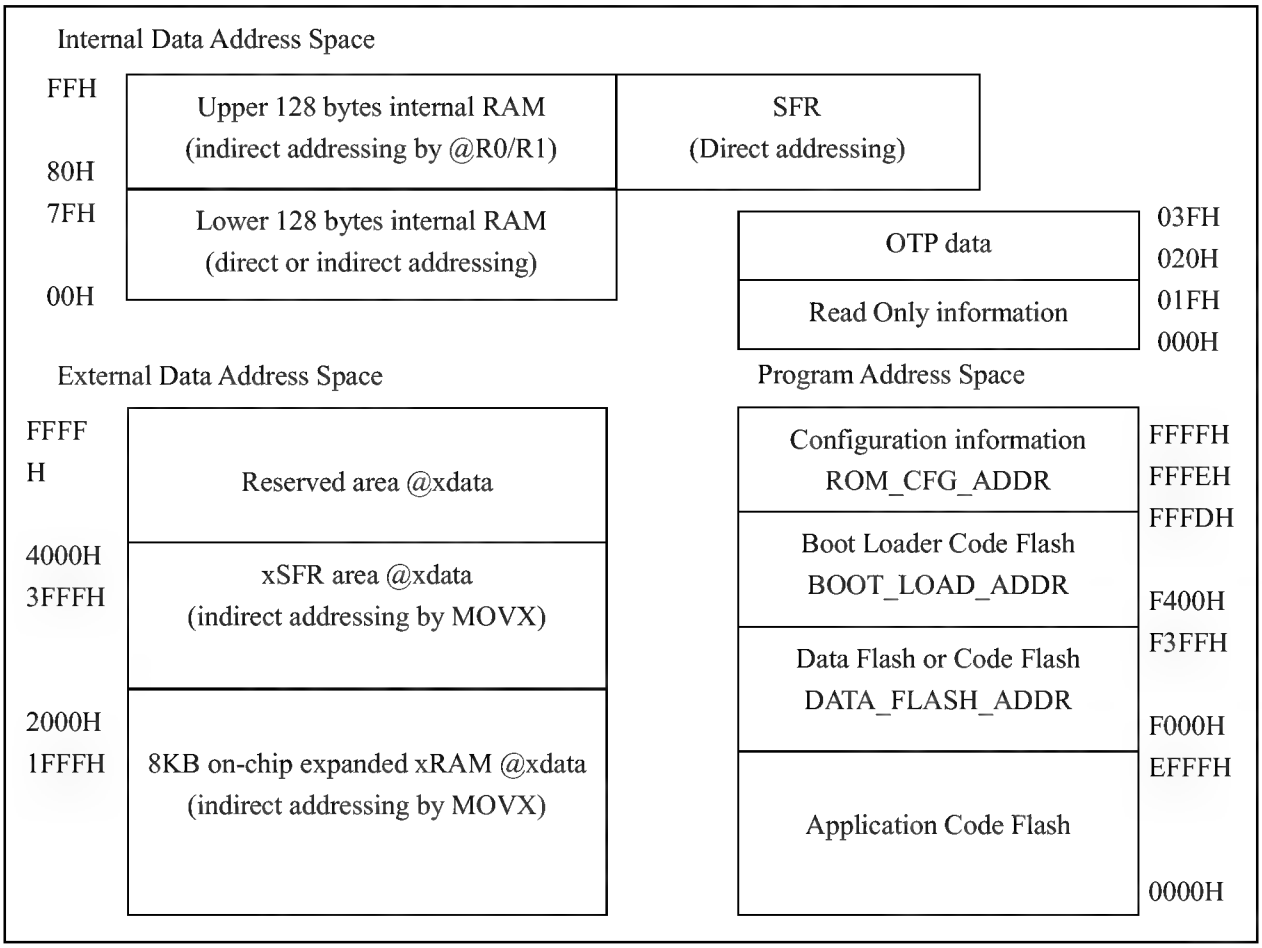
(5). Alternatively, writing any value to the register can prematurely terminate the safe mode

6. Memory structure

6.1 Memory space

CH555 addressing space is divided into Program Address Space, Internal Data Address Space and External Data Address Space, read-only and OTP space.

Figure 6.1 Memory structure diagram



6.2 Program address space

The program address space is 64KB in total, as shown in Figure 6.1, all is used for flash-ROM, including Code Flash area to save command codes, Data Flash area to save non-volatile data, and Configuration Information area to configure information.

Data Flash (EEPROM) address ranges from F000h to F3FFH, supports single-byte read (8 bits), single-byte write (8 bits), block write (1 ~ 64 bytes), block erase (64 bytes) operations. The data remains unchanged after power-down of chip, and it can also be used as Code Flash.

Code Flash includes the application code for the low address area and the boot loader code for the high address area, or these two areas and Data Flash may be combined to save single-application codes.

Configuration information has 16 bits of data, set by programmer as required, refer to Table 6.1.

Table 6.2 flash-ROM configuration information description

Bit address	Bit name	Description	Recommended value
15	Code_Protect	Code and data protection mode in flash-ROM: 0- Allow read; 1- Forbid the programmer to read, and keep program secret	0/1
14	No_Boot_Load	Enable BootLoader start mode: 0- Start from the application from 0000h address; 1- Start from the boot loader from F400h address	1
13	En_Long_Reset	Extra delay reset during enable power on reset: 0-standard short reset; 1-wide reset, extra 44mS reset time is added	0
12	En_P71_RESET	Enable P7.1 as manual reset input pin: 0- Disable; 1 - Enable RST#	0
11		Reserved	0
10		Reserved	0
9	Must_1	(Automatically set to 1 by programmer as required)	1
8	Must_0	(Automatically set to 0 by programmer as required)	0
[7:3]	All_0	(Automatically set to 00000b by programmer as required)	00000b
[2:0]	LV_RST_VOL (Vpot)	Select the threshold voltage of power supply low voltage detection reset module LVR (5% error): 000: Select 2.5V; 001: Select 2.7V; 010: Select 2.9V; 011: Select 3.1V; 100: Select 3.9V; 101: Select 4.1V; 110: Select 4.3V; 111: Select 4.5V.	000b

6.3 Data address space

The internal data address space has 256 bytes in total, as shown in Figure 6.1, all has been used for SFR and iRAM. And iRAM is used for stack and fast temporary data storage, and can be subdivided into the working registers R0-R7, bit variable bdata, byte variable data and idata, etc.

External data address space has 64KB in total, as shown in Figure 6.1. Except that part of it is used to expand 16KB on-chip xRAM and xSFR, the remaining 4000h to FFFFh address range is reserved.

Read-only information and OTP data each has 32 bytes, as shown in Figure 6.1, and needs to be accessed through a dedicated operation.

6.4 flash-ROM register

Table 6.4 flash-ROM operation registers

Name	Address	Description	Reset value
ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HI	8Eh	ROM_DATA_HL and ROM_DATA_HH constitute a 16-bit SFR	xxxxh
ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxh
ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxh
ROM_STATUS	86h	flash-ROM status register (read only)	00h
ROM_CTRL	86h	flash-ROM control register (write only)	00h
ROM_ADDR_H	85h	flash-ROM address register high byte	xxh
ROM_ADDR_L	84h	flash-ROM address register low byte	xxh
ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh
ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LO	84h	ROM_DATA_LL and ROM_DATA_LH constitute a 16-bit SFR	xxxxh

flash-ROM address register (ROM_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_ADDR_H	RW	flash-ROM address high byte	xxh
[7:0]	ROM_ADDR_L	RW	flash-ROM address low byte	xxh

flash-ROM data register (ROM_DATA_HI, ROM_DATA_LO):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DATA_HH	RO	High byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_HL	RO	Low byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_LH	RO	High byte of flash-ROM data register low word (16 bits)	xxh
[7:0]	ROM_DATA_LL	RO	Low byte of flash-ROM data register low word (16 bits)	xxh

Buffer mode register for flash-ROM erase/program operation (ROM_BUF_MOD):

Bit	Name	Access	Description	Reset value
7	bROM_BUF_BYTE	RW	Buffer mode for flash-ROM erase/program operation: If the bit is 0, select data block program mode, and the data to be written is stored in the pointed xRAM by DPTR. During programming, CH555 will automatically fetch data from xRAM in sequence and temporarily store it in ROM_DAT_BUF and then write into flash-ROM. It supports data length of 1-byte to 64-byte, and the actual length =MASK_ROM_ADR_END-ROM_ADDR_L[5:0]+1; If the bit is 1, select single-byte program or 64-byte block erase mode, and the data to be written is directly stored in ROM_DAT_BUF.	x
6	Reserved	RW	Reserved	x
[5:0]	MASK_ROM_ADDR	RW	In flash-ROM data block program mode, it is the lower 6 bits of the end address of the flash-ROM block program operation (including this address). In flash-ROM single-byte program or 64-byte erase mode, it is reserved and recommended to be 00h.	xxh

Data buffer register for flash-ROM erase/program operation (ROM_DAT_BUF):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DAT_BUF	RW	Data butter register for flash-ROM erase/program operation	xxh

flash-ROM control register (ROM_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

flash-ROM status register (ROM_STATUS):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	1
6	bROM_ADDR_OK	RO	flash-ROM operation address valid status bit: 0: Invalid. 1: Address is valid	0
[5:2]	Reserved	RO	Reserved	0000b
1	bROM_CMD_ERR	RO	flash-ROM operation command error status bit: 0: Command is valid. 1: Unknown command or overtime	0
0	Reserved	RO	Reserved	0

6.5 flash-ROM operation steps

1. Erase flash-ROM, and change all data bits in the target block to 0:

(1). Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds to code or data);
(3). Set the address register (ROM_ADDR), write 16-bit target address, actually only the higher 10 bits are valid;
(4). Set the buffer mode register (ROM_BUF_MOD) for erase/program operation to be 80h, and select 64-byte block erase mode;
(5). Optional, set the data buffer register (ROM_DAT_BUF) for erase/program operation to be 00h;
(6). Set the operation control register (ROM_CTRL) to be 0A6h, execute block erase operation and the program automatically pauses during operation;
(7). After the operation is completed, the program will resume running. At this time, if you inquire the status register (ROM_STATUS) to know the status of the operation. If more than one block needs to be erased, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged;
(8). Re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0);

2. Write flash-ROM in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1). Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds to code or data);
(3). Set the address register (ROM_ADDR), write 16-bit target address;
(4). Set the buffer mode register (ROM_BUF_MOD) for erase/program operation to be 80h, and select single-byte program mode;
(5). Set the data buffer register (ROM_DAT_BUF) for erase/program operation as the byte data to be written;
(6). Set the operation control register ROM_CTRL as 09Ah, execute write operation, and the program automatically pauses during operation;
(7). After the operation is completed, the program will resume running. At this time, if you inquire the status register ROM_STATUS, you can check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7), and the sequence of step (3), (4), and (5) can be exchanged;
(8). Re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0);

3. Block write flash-ROM, change some data bits in multiple target bytes from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1). Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds to code or data);
(3). Set the address register (ROM_ADDR), write 16-bit start target address, for example, 1357h;
(4). Set the buffer mode register (ROM_BUF_MOD) for erase/program operation as the lower 6 bits of the end target address (included), and such end address should be greater than or equal to the start

target address of ROM_ADDR_L[5:0], select data block program mode, for example, if the end address is 1364h, ROM_BUF_MOD should be set to 24h (64h&3Fh), and the calculated number of bytes of the data block =0Dh;

(5). In xRAM, allocate a buffer area based on the alignment in 64 bytes, for example 0580h～05BFh, specify the offset address in such buffer area with the lower 6 bits of the start target address, obtain the xRAM buffer start address of this data block program operation, store the data block to be written from the xRAM buffer start address, and set the xRAM buffer start address to DPTR, e.g. DPTR=0580h+(57h&3Fh)=0597h, actually only the xRAM of 0597h ~ 05A4h address is used in this program operation;

(6). Set the operation control register (ROM_CTRL) as 09Ah, execute write operation, and the program automatically pauses during operation;

(7). After the operation is completed, the program will resume running. At this time, if you inquire the status register (ROM_STATUS), you can check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7), and the sequence of step (3), (4), and (5) can be exchanged;

(8). Re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0);

4. Read flash-ROM:

Directly use MOVC commands, or read the code or data of the target address through the pointer to the program address space.

5. Write OTP data area in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):

(1). Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bDATA_WE);

(3). Set the address register (ROM_ADDR),write target address (20h～3Fh), actually only the higher 4 bits of the lower 6 bits are valid;

(4). Set the buffer mode register (ROM_BUF_MOD) for erase/program operation to be 80h, and select single-byte program mode;

(5). Set the data buffer register (ROM_DAT_BUF) for erase/program operation as the byte data to be written;

(6). Set the operation control register (ROM_CTRL) as 099h, execute write operation, and the program automatically pauses during operation;

(7). After the operation is completed, the program will resume running. At this time, if you inquire the status register ROM_STATUS, you can check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7), and the sequence of step (3), (4), and (5) can be exchanged;

(8). Re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0);

6. Read the ReadOnly information zone or OTP data zone in unit of 4 bytes:

(1). Set the address register (ROM_ADDR), write target address based on the alignment in 4 bytes (00h～3Fh), actually only the lower 6 bits are valid;

(2). Set the operation control register (ROM_CTRL) as 08Dh, execute read operation, and the program automatically pauses during operation;
(3). After the operation is completed, the program will resume running. At this time, if you inquire the status register (ROM_STATUS), you can check the status of the operation;
(4). Obtain 4-byte data from ROM_DATA_HI and ROM_DATA_LO in flash-ROM data register.

7. Notes: it is recommended that flash-ROM/EEPROM is erased/programmed only at the ambient temperature of -20℃ ~ 85℃. If the erase/program operation is conducted beyond the above temperature range, it will be normal in general, but there may be the possibility of reducing data retention ability TDR and reducing the number of erase/program NEPCE or even affecting the accuracy of data.

6.6 On-board program and ISP download

When the configuration information Code_Protect=0, the code and data in CH555 flash-ROM can be read and written by an external programmer through the synchronous serial port. When the configuration information Code_Protect=1, the code and data in the flash-ROM are protected and cannot be read out, but can be erased, and the code protection will be removed after erased and powered on again.

When the CH555 is preset with BootLoader program, it supports various ISP download ways such as USB or asynchronous serial port to load the applications. But in the absence of BootLoader program, CH555 can only be written the BootLoader program or application by an external dedicated programmer. To support on-board program, 4 connecting pins between CH555 and the programmer should be reserved in the circuit. The necessary connecting pins are at least P1.4, P1.6 and P1.7.

Table 6.6.1 Connecting Pin to Programmer

Pin	GPIO	Pin description
VDD	VDD	Chip supply required to be controlled in programming state
SCS	P1.4	Chip select input pin in programming state (necessary), high level by default, active at low level
SCK	P1.7	Clock input pin in programming state (necessary)
MISO	P1.6	Data output pin in programming state (necessary)

6.7 Unique ID number of chip

Each MCU has a unique ID number when it is delivered from the factory, namely the chip identification number. This ID data and its checksum have 8 bytes in total, stored in area with offset address of 10h of the read-only information zone, please refer to the C Program Language example program for specific operations.

Table 6.7.1 Chip ID address table

Offset address	ID data description
10h, 11h	ID first word data, correspond to the lowest byte and the secondary lowest byte of ID number
12h, 13h	ID secondary word data, correspond to the secondary high byte and high byte of ID number
14h, 15h	ID last word data, correspond to the secondary highest byte and the highest byte of the 48-bit ID number
16h, 17h	16-bit cumulative sum of ID first word, secondary word, last word data, used for ID

	check

The ID number can be used with the downloading tools to encrypt the target program. For general application, only the first 32 bits of the ID number are required.

7. Power control, sleep and reset

7.1 External power input

The CH555 has built-in low dropout voltage regulator (LDO) from 5V to 3.3V, and the generated 3.3V power supply is used in USB and other modules. CH555 supports external 5V or 3.3V or even 2.8V supply voltage input. Refer to the following table for the two supply voltage input modes.

External supply voltage	VDD pin voltage: external voltage 2.8V~5V	V33 pin voltage: internal USB voltage 3.3V (Notes: V33 will be automatically short connected to VDD during sleep)
3.3V or 2.8V including less than 3.6V	Input external 3.3V voltage to I/O and voltage regulator, The decoupling capacitance no less than 0.1uF must be connected to the ground	Short connect VDD input as the internal USB power, The decoupling capacitance no less than 0.1uF must be connected to the ground
5V including more than 3.6V	Input external 5V voltage to I/O and voltage regulator, The decoupling capacitance no less than 0.1uF must be connected to the ground	Internal voltage regulator 3.3V output And 3.3V internal USB power supply input, The decoupling capacitance no less than 0.1uF must be connected to the ground

After power on or system reset, CH555 is in running state by default. On the premise that the performance meets the requirements, the power consumption can be reduced during operation by appropriately reducing the clock frequency of the system. When CH555 does not need to be run at all, PD in PCON can be set to enter the sleep state. In the sleep state, external waking can be conducted via USB, UART0, UART1, SPI0 and part of GPIOs.

7.2 Power supply and sleep control register

Table 7.2.1 Power supply and sleep control registers

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset keep register	00h
POWER_CFG	BAh	Power control configuration register	0xh
WAKE_CTRL	A9h	Sleep wake-up control register	00h
PCON	87h	Power control register	10h
CMP_DCDC	21EBh	Comparator and DC-DC control register	00h

Watchdog count register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Current count of watchdog, it will overflow when the count is full from 0FFh to 00h, and it will automatically set the interrupt flag (bWDOG_IF_TO) to 1 during overflow	00h

Reset keep register (RESET_KEEP):

Bit	Name	Access	Description	Reset value
[7:0]	RESET_KEEP	RW	Reset keep register. The value can be modified manually and will not be affected by any other reset except for power on reset	00h

Power control configuration register (POWER_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bPWR_DN_MODE	RW	Select sleep power off mode: 0: Select power off/deep sleep mode, saving more power but wake up slowly; 1: Select standby/normal sleep mode, wake up quickly	0
6	bCMP_RESULT	RO	Result real-time output bit of voltage comparator 0: Input voltage is lower than the reference voltage. 1: Input voltage is higher than the reference voltage	0
5	bLV_RST_OFF	RW	OFF control of low voltage reset detection module 0: Enable supply voltage detection and generate reset signal at low voltage. 1: Disable the low voltage detection	0
4	bLDO_3V3_OFF	RW	OFF control of USB power regulator LDO (automatic OFF during sleep): 0: 3.3V voltage is generated by VDD power supply for USB and other modules; 1: Disable LDO and internally short connect V33 to VDD	0
3	bLDO_CORE_VOL	RW	Core voltage mode: 0: Normal voltage mode; 1: Boost voltage mode, with better performance and support higher system clock frequency	0
[2:0]	MASK_ULLDO_VOL	RW	Select data keep supply voltage in power off/deep sleep mode: 000- select 1.5V; 001-select 1.57V; 010- select 1.64V; 011-select 1.71V; 100- select 1.78V; 101-select 1.85V; 110- select 1.92V; 111-select 1.99V. The above values are for reference only and not recommended to modify.	xxxb

Sleep wake-up control register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0

6	bWAK_RXD1_LO	RW	UART1 receive input low level wake-up enable If the bit is 0, wake-up disabled. Select either pin RXD1 or pin RXD1_ based on bUART1_PIN_X=0/1	0
5	bWAK_P1_5_LO	RW	P1.5 low level wake-up enable If the bit is 0, wake-up disabled.	0
4	bWAK_P1_4_LO	RW	P1.4 low level wake-up enable If the bit is 0, wake-up disabled.	0
3	bWAK_BY_USB	RW	USB event wake-up enable If the bit is 0, wake-up disabled.	0
2	bWAK_P3_3_LO	RW	P3.3 low level wake-up enable If the bit is 0, wake-up disabled.	0
1	bWAK_INT0_EDGE	RW	INT0 edge change wake-up enable If the bit is 0, wake-up disabled. Select either pin INT0 or pin INT0_ based on bINT0_PIN_X=0/1	0
0	bWAK_RXD0_LO	RW	UART0 receives input low level wake-up enable If the bit is 0, wake-up disabled. Select either pin RXD0 or pin RXD0_ based on bUART0_PIN_X=0/1	0

Other signal sources that can wake up the chip include:

When bP4_IE_LEVEL is 1, the level change on any pin of P4.0～P4.7 will wake up the chip.

When bP2L_IE_LEVEL is 1, the level change on any pin of P2.0～P2.3 will wake up the chip.

When bP1L_IE_LEVEL is 1, the level change on any pin of P1.0～P1.3 will wake up the chip.

When bP0_IE_LEVEL is 1, the level change on any pin of P0.0～P0.7 will wake up the chip.

When En_P71_RESET is 1, enable RST#, and low level of P7.1 pin will wake up and reset the chip.

Power control register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	When UART0 baud rate is generated by Timer1, select communication baud rate of UART0 mode 1, 2 and 3: 0-slow mode; 1-fast mode	0
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	RO	Last reset flag high bit of chip	0
4	bRST_FLAG0	RO	Last reset flag low bit of chip	1
3	GF1	RW	General flag bit 1 User-defined. Cleared and set by software	0
2	GF0	RW	General flag bit 0 User-defined. Cleared and set by software	0
1	PD	RW	Sleep mode enable. Sleep after set 1. Automatically cleared by hardware after wake-up. It is strongly recommended to turn off the global interrupt before sleep (EA=0).	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Last reset flag description

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset, source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1)
0	1	Power on reset or low voltage detection reset, source: VDD pin voltage is lower than detection level
1	0	Watchdog reset, source: bWDOG_EN=1 and watchdog timeout overflows
1	1	External pin manual reset, source: En_P71_RESET=1 and P71 input low level

Comparator and DC-DC control register (CMP_DCDC):

Bit	Name	Access	Description	Reset value
7	bDCDC_ACT	RO	DC-DC output activation status (read only): 0: Idle. 1: Driver is being activated.	0
6	bDCDC_PIN	RW	DC-DC output permission and polarity selection: 0: Only DCO pin outputs bDCDC_ACT signal. 1: DCO pin outputs bDCDC_ACT reverse polarity signal, and P6.4 pin outputs bDCDC_ACT signal whose polarity is controlled by P6_OUT_PU[4]. When P6_OUT_PU[4]=0, output positive polarity. When P6_OUT_PU[4]=1, output negative polarity	0
[5:4]	MASK_DCDC_FREQ	RW	When MASK_CMP_VREF!=000, select reference frequency of DC-DC controller (the actual maximum output frequency is 1/3 of the reference frequency): 00- turn off DC-DC controller; 01- select 3MHz reference frequency; 10- select 1.5MHz reference frequency; 11- select 750KHz reference frequency. When MASK_CMP_VREF=000, directly control bDCDC_ACT status: 00 set bDCDC_ACT=0; 01/10/11 set bDCDC_ACT=1	00b
3	bCMP_PIN	RW	Input voltage selection of voltage comparator (positive phase input): 0: Select VDD power supply through partial voltage input. 1: Select the analog input channel through the partial voltage connection, share with ADC, and select the external input pin by ADC_CHAN, and bADC_EN=1	0
[2:0]	MASK_CMP_VREF	RW	Reference voltage selection of comparator (inverted input):	000b

			000- turn off comparator; 001- select internal reference voltage, about 1.2V; 010- select 3.3V; 011-select 5V; 100-select 5.4V; 101- select 5.8V; 110-select 6.2V; 111-select 6.6V	

The inverted input of the voltage comparator CMP is selected by MASK_CMP_VREF for the reference voltage, actually the reference voltage remains unchanged, while adjust the resistance partial voltage ratio of the positive phase input to simulate the selection equivalent to the reference voltage. Due to the existence of the partial voltage, the impedance of the positive phase input is between 50KΩ and 150KΩ, and the CMP is generally used for supply voltage monitor and DC-DC control.

7.3 Reset control

CH555 has 5 reset sources: power on reset and supply low voltage detection reset, external reset, software reset and watchdog reset. The last three are thermal reset.

7.3.1 Power-on reset and supply low voltage detection reset

The power on reset (POR) is generated by the on-chip power on detection circuit, and remain the reset state via the hardware automatic delay of Tpor. After delay, CH555 will run.

Supply low voltage detection reset (LVR) is generated by the on-chip voltage detection circuit. The LVR circuit continuously monitors the supply voltage of VDD pin. When it is lower than the detection level Vpot, the low voltage reset will be generated, and the hardware will automatically delay Tpor to remain the reset state. After delay, CH555 will run.

Only power on reset and supply low voltage detection reset can enable CH555 to reload configuration information and clear RESET_KEEP, other thermal resets do not affect.

7.3.2 External reset

The external reset is generated by the low level applied to the RST# pin. The reset process is triggered when the configuration information En_P71_RESET is 1, and the time of low level kept on RST# pin is greater than Trst. When the external low level signal is canceled, the hardware will automatically delay Trdl to remain the reset state. After the delay, CH555 will execute from address 0.

Notes: RST# pin is also the XO pin of the external crystal oscillator. It is necessary to avoid adding additional capacitance or introducing interference with long line.

7.3.3 Software reset

CH555 supports internal software reset, so that CPU can be actively reset and re-run without external intervention. Set bSW_RESET in global configuration register GLOBAL_CFG to 1 for software reset, and automatically delay Trdl to remain reset state. After the delay, CH555 executes from address 0, and bSW_RESET bit can be automatically cleared by hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 after reset will indicate software reset. When bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 will remain the previous reset flag rather than generating a new one.

For chip with ISP boot loader, after power on reset, firstly run the boot loader, and the program will reset the chip via software as needed to switch to application state. Such software reset only causes reset of bBOOT_LOAD, and does not affect bRST_FLAG1/0 state (because bBOOT_LOAD=1 before reset), so

when switching to application state, bRST_FLAG1/0 will still indicate power on reset state.

7.3.4 Watchdog reset

Watchdog reset is generated when the watchdog timer overflows. The watchdog timer is an 8-bit counter, whose clock frequency of count is Fsys/131072. And the overflow signal will be generated when the count reaches 0FFh to 00h.

The watchdog timer overflow signal triggers the interrupt flag (bWDOG_IF_TO) as 1, which is automatically cleared when WDOG_COUNT is reloaded or enterring the corresponding interrupt service program.

Different timing cycles Twdc can be realized by writing different count initial values to WDOG_COUNT. At the system clock frequency of 12MHz, the watchdog timing cycle Twdc is about 2.8 s when 00h is written, and about 1.4 s when 80h is written.

If bWDOG_EN=1 when watchdog timer overflows, watchdog reset will be generated and automatically delay Trdl to remain the reset state. After the delay, CH555 will execute from address 0.

When bWDOG_EN=1, to avoid being reset by watchdog, WDOG_COUNT must be reset timely to avoid its overflow.

8. System clock

8.1 Clock block diagram

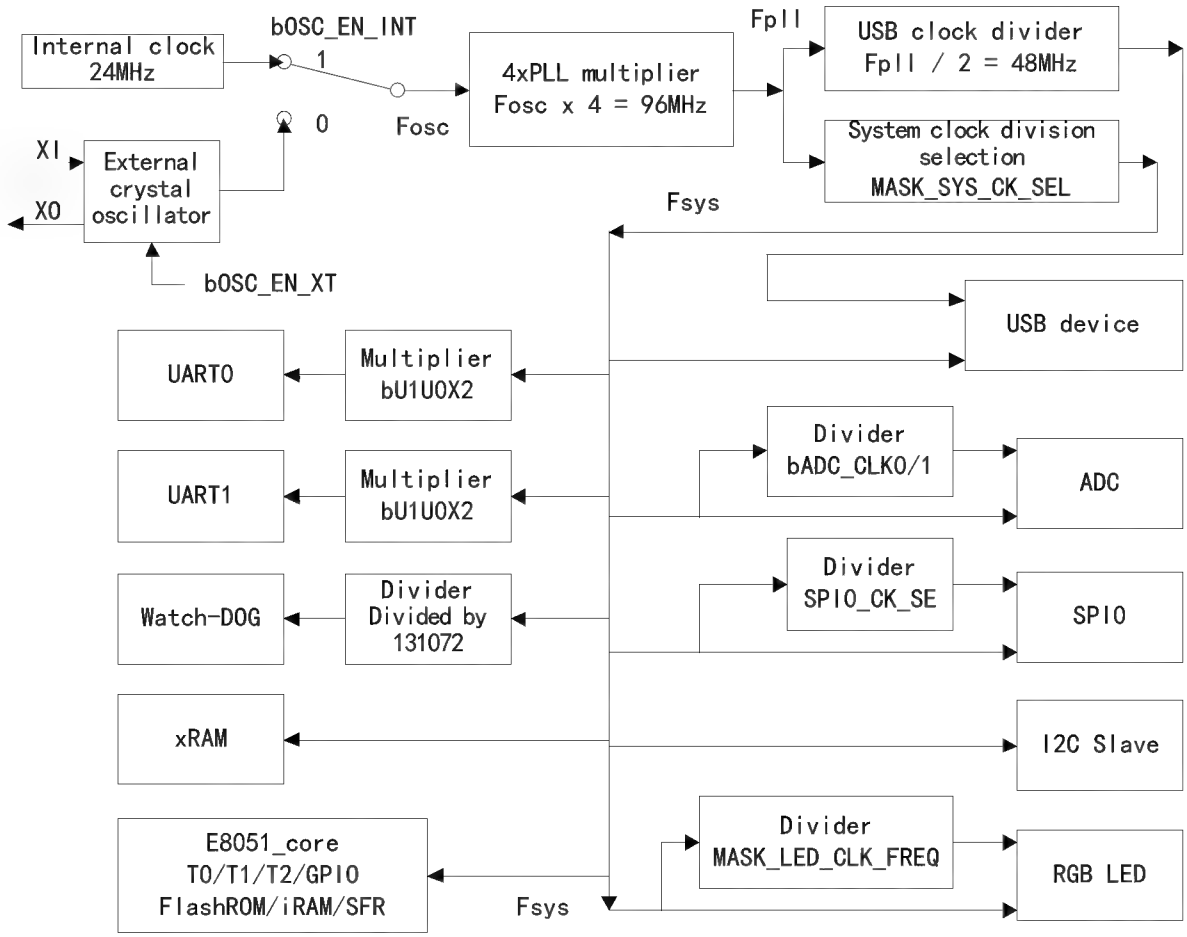


Figure 8.1.1 Clock System and Structure Chart

After the internal clock or external clock is alternatively selected as the original clock (Fosc), Fpll high frequency clock is generated after PLL frequency multiplier, and finally the system clock (Fsys) and USB module clock (Fusb4x) are respectively obtained via the two groups of frequency dividers. System clock (Fsys) is directly provided for each module of CH555.

8.2 Register description

Table 8.2.1 Clock control register

Name	Address	Description	Reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System clock configuration register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bOSC_EN_INT	RW	Internal clock oscillator enable 1: Internal clock oscillator enabled, and select internal clock. 0: Internal clock oscillator disabled, and select external crystal oscillator to provide the clock.	1
6	bOSC_EN_XT	RW	External crystal oscillator enable 1: P7.0/P7.1 pin used as XI/XO and the oscillator enabled. A quartz crystal or ceramic oscillator needs to be externally connected between XI and XO. 0: External oscillator disabled.	0
5	bWDOG_IF_TO	RO	Watch dog timer interrupt flag bit 1: Interrupt, triggered by timer overflow signal. 0: No interrupt. The bit is automatically cleared when watchdog count register (WDOG_COUNT) is reloaded or after enterring the corresponding interrupt service program.	0
[4:3]	Reserved	RO	Reserved	00b
[2:0]	MASK_SYS_CK_SEL	RW	System clock frequency selection Refer to Table 8.2.2	011b

Table 8.2.2 System clock frequency selection table

MASK_SYS_CK_SEL	Fsys	Relation with crystal frequency Fxt	Fsys when Fosc=24MHz
000b	Fpll / 512	Fxt / 128	187.5KHz
001b	Fpll / 128	Fxt / 32	750KHz
010b	Fpll / 32	Fxt / 8	3MHz
011b	Fpll / 8	Fxt / 2	12MHz
100b	Fpll / 6	Fxt / 1.5	16MHz
101b	Fpll / 4	Fxt / 1	24MHz

110b	Fpll / 3	Fxt / 0.75	32MHz
111b	Fpll / 2	Fxt / 0.5	Reserved (48MHz only for test)

Note: It is recommended to use frequencies of 32MHz and below. If 48MHz is strongly needed, it is recommended to set bLDO_CORE_VOL to 1 first.

8.3 Clock configuration

The internal clock is used by default after CH555 is powered on, and the internal clock frequency is 24MHz. The internal clock or external crystal oscillator clock can be selected through CLOCK_CFG. If the external crystal oscillator is turned off, then XI and XO pins can be used as P7.0 and P7.1 common I/O ports respectively. If an external crystal oscillator is used to provide clock, a crystal should be cross connected between XI and XO pins, and the oscillator capacitor should be connected to GND between XI and XO pins respectively. If the clock signal is input directly from the outside, it should be input from XI pin, with XO pin suspended.

Original clock frequency, Fosc = bOSC_EN_INT ? 24MHz : Fxt
PLL frequency, Fpll = Fosc * 4
USB clock frequency, Fusb4x = Fpll / 2
The system clock frequency Fsys is obtained by Fpll frequency division, refer to Table 8.2.2.
In default state after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, and Fsys=12MHz.

Steps for switching to the external crystal oscillator to provide clock are as follows:
(1). Make P7.0(XI) pin output low level (used for discharge to crystal oscillator capacitor, ensure that P7.1 is not at low level to avoid reset)
P7 = P7 & 0xF0 | 0x06 ; // Before enabling external crystal oscillator, P7.0 is at low level and P7.1 is in pull-up state
(2). Enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
(3). Set bOSC_EN_XT in CLOCK_CFG to 1 with "or by bit" operation, other bits remain unchanged, to enable crystal oscillator;
(4). Delay several milliseconds, usually 1mS ~ 10mS, wait for the crystal oscillator to work steadily;
(5). Re-enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
(6). Reset bOSC_EN_INT in CLOCK_CFG to 0 with "and by bit" operation, other bits remain unchanged, to switch to external clock;
(7). Terminate safe mode, write any value into SAFE_MOD to prematurely terminate the safe mode.

Steps for modifying the system clock frequency are as follows:
(1). Enter the safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
(2). Write a new value to CLOCK_CFG;
(3). Terminate safe mode, write any value into SAFE_MOD to prematurely terminate the safe mode.

Remarks:
(1). If the USB module is used, Fusb4x must be 48MHz. And when USB is used, Fsys is not less than 6MHz.
(2). For USB device applications with higher requirements, it is recommended to switch to the external crystal oscillator to provide the clock.
(3). A lower system clock frequency Fsys is preferred to be used, to reduce the system dynamic power

consumption and widen the operating temperature range.

9. Interrupt

CH555 supports 14 sets of interrupt signal sources, including 6 sets of interrupts compatible with the standard MCS51: INT0, T0, INT1, T1, UART0, T2, and 8 sets of extended interrupts: SPI0, USB, ADC, UART1, LED/I2C, GPIO, WDOG, in which GPIO interrupt can be selected from multiple I/O pins.

Interrupt service programs are advised to be as compact as possible, try not to call functions and subroutines as well as read/write xdata variables and code constants.

9.1 Register rescription

Table 9.1.1 Interrupt vector table

Interrupt sources	Entry address	Interrupt No.	Description	Default priority sequence
INT_NO_INT0	0x0003	0	External interrupt 0	High priority ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ Low priority
INT_NO_TMR0	0x000B	1	Timer0 interrupt	
INT_NO_INT1	0x0013	2	External interrupt 1	
INT_NO_TMR1	0x001B	3	Timer1 interrupt	
INT_NO_UART0	0x0023	4	UART0 interrupt	
INT_NO_TMR2	0x002B	5	Timer2 interrupt	
INT_NO_SPI0	0x0033	6	SPI0 interrupt	
INT_NO_USB	0x003B	7	USB interrupt	
None	0x0043	8	Reserved	
INT_NO_ADC	0x004B	9	ADC interrupt	
INT_NO_UART1	0x0053	10	UART1 interrupt	
INT_NO_PWM_I2C	0x005B	11	Data is distinguished based on I2CX_INT after interrupt, and it is the "or" of the following 2 interrupts: RGB LED interrupt (when bLED_IE_INHIB=1); I2CS interrupt (when bI2CS_IE_*=1);	
INT_NO_GPIO	0x0063	12	GPIO Interrupt	
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 Interrupt related registers

Name	Address	Description	Reset value
IP_EX	E9h	Extend interrupt priority control register	00h
IE_EX	E8h	Extend interrupt enable register	00h
GPIO_IE	B2h	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
IE	A8h	Interrupt enable register	00h

interrupt enable register (IE):

Bit	Name	Access	Description	Reset value
7	EA	RW	Global interrupt enable control bit 1: Interrupt enabled when E_DIS is 0, 0: Interrupt disabled.	0
6	E_DIS	RW	Global interrupt disable control bit 1: Interrupt disabled. 0: Interrupt enabled when EA is 1,. This bit is usually used for temporary disable interrupt during flash-ROM operation.	0
5	ET2	RW	Timer2 interrupt enable bit 1: T2 interrupt enabled. 0: T2 interrupt disabled.	0
4	ES	RW	UART0 interrupt enable bit 1: UART0 interrupt enabled. 0: UART0 interrupt disabled.	0
3	ET1	RW	Timer1 interrupt enable bit 1: T1 interrupt enabled. 0: T1 interrupt disabled.	0
2	EX1	RW	External interrupt 1 enable bit 1: INT1 interrupt enabled. 0: INT1 interrupt disabled.	0
1	ET0	RW	Timer0 interrupt enable bit 1: T0 interrupt enabled. 0: T0 interrupt disabled.	0
0	EX0	RW	External interrupt 0 enable bit 1: INT0 interrupt enabled. 0: INT0 interrupt disabled.	0

Extend interrupt enable register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable bit 1: WDOG interrupt enabled; 0: WDOG interrupt disabled.	0
6	IE_GPIO	RW	GPIO interrupt enable bit 1: GPIO_IE interrupt enabled; 0: GPIO_IE interrupt disabled.	0
5	IE_PWM_I2C	RW	RGB LED and I2CS interrupt enable bit 1: RGB LED and I2CS interrupt enabled. 0: RGB LED and I2CS interrupt disabled.	0
4	IE_UART1	RW	UART1 interrupt enable bit 1: UART1 interrupt enabled. 0: UART1 interrupt disabled.	0
3	IE_ADC	RW	ADC interrupt enable bit 1: ADC interrupt enabled.	0

			0: ADC interrupt disabled.	
2	Reserved	RO	Reserved	0
1	IE_USB	RW	USB interrupt enable bit 1: USB interrupt enabled. 0: USB interrupt disabled.	0
0	IE_SPI0	RW	SPI0 interrupt enable bit 1: SPI0 interrupt enabled. 0: SPI0 interrupt disabled.	0

GPIO interrupt enable register (GPIO_IE), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: 0: Level interrupt mode selected. If GPIO pin inputs valid level, bIO_INT_ACT will be 1 and always request interrupt. If GPIO inputs invalid level, bIO_INT_ACT is 0 and cancels interrupt request. 1: Edge interrupt mode selected. When GPIO pin inputs valid edge, interrupt flag bIO_INT_ACT will be generated and interrupt is requested. The interrupt flag cannot be cleared by software and can only be cleared automatically when reset or in level interrupt mode or when enterring the corresponding interrupt service program	0
6	bIE_RXD1_LO	RW	1: UART1 receive pin interrupt enabled (active at low level in level mode, active at falling edge in edge mode). 0: Disabled. Select either RXD1 or RXD1_ based on bUART1_PIN_X=0/1	0
5	bIE_P1_5_LO	RW	1: P1.5 interrupt enabled (active at low level in level mode, active at falling edge in edge mode). 0: Disabled.	0
4	bIE_P1_4_LO	RW	1: P1.4 interrupt enabled (active at low level in level mode, active at falling edge in edge mode). 0: Disabled.	0
3	bIE_P0_3_LO	RW	1: P0.3 interrupt enabled (active at low level in level mode, active at falling edge in edge mode). 0: Disabled.	0
2	bIE_P5_3X5X7	RW	1: P5.3, P5.5 and P5.7 level change interrupt enabled. 0: Disabled.	0
1	bIE_P7_1_LO	RW	When bOSC_EN_XT=0, if the bit is 1, P7.1 interrupt enabled (active at low level in level mode, active at falling edge in edge mode). If the bit is 0, disabled.	0
1	bIE_CMP_RES_LO	RW	When MASK_CMP_VREF!=000, if the bit is 1, voltage comparator result bCMP_RESULT interrupt enabled (active when below the reference voltage in	0

			level mode, and active when from above the reference voltage to below the reference voltage in edge mode). If the bit is 0, disabled.	
0	bIE_RXD0_LO	RW	1: UART0 receiving pin interrupt enabled (active at low level in level mode, active at falling edge in edge mode). 0: Disabled. Select either RXD0 or RXD0_ pin based on bUART0_PIN_X=0/1	0

Other signal sources that can generate GPIO interrupt include:

When bP4_IE_LEVEL is 1, the level change on any pin of P4.0～P4.7 will generate GPIO interrupt.

When bP2L_IE_LEVEL is 1, the level change on any pin of P2.0～P2.3 will generate GPIO interrupt.

When bP1L_IE_LEVEL is 1, the level change on any pin of P1.0～P1.3 will generate GPIO interrupt.

When bP0_IE_LEVEL is 1, the level change on any pin of P0.0～P0.7 will generate GPIO interrupt.

Interrupt priority control register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	Flag bit for high-priority interrupt in progress	0
6	PL_FLAG	RO	Flag bit for low-priority interrupt in progress	0
5	PT2	RW	Timer2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 interrupt priority control bit	0
1	PT0	RW	Timer0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 interrupt priority control bit	0

Extend interrupt priority control register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nesting level flag bit 0: No interrupt, or 2-level interrupt nested. 1: Currently, 1-level interrupt nested	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWM_I2C	RW	RGB LED and I2CS interrupt priority control bit	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	Reserved	RO	Reserved	0
1	bIP_USB	RW	USB interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

IP and IP_EX registers are used to set the interrupt priority, if a bit is set to 1, then the corresponding interrupt source is set to be high priority. If a bit is cleared to 0, then the corresponding interrupt source is set to be low priority. For the interrupt source at the same level, the system has a priority sequence by default, as shown in Table 9.1.1. And the combination of PH_FLAG and PL_FLAG represents the priority of the current interrupt.

Table 9.1.3 Current interrupt priority states

PH_FLAG	PL_FLAG	Current interrupt priority state
0	0	No interrupt now
0	1	Low priority interrupt is executing at present
1	0	High priority interrupt is executing at present
1	1	Unexpected state, unknown error

10. I/O Port

10.1 GPIO introduction

CH555 provides up to 58 I/O pins, some of which have alternate functions. The P0～P4 input/output ports can be addressed in bits.

If the pin is not configured with alternate functions, it is a general-purpose I/O pin by default. When used as a general-purpose digital I/O, all I/O ports have a real "read-modify-write" function, that allows SETB or CLR and other bit operation commands to independently change the direction of some pins or port level.

10.2 GPIO register

All registers and bits in this section are represented in a generic format: a lowercase "n" represents the serial number of ports (n=0, 1, 2, 3, 4)), a lowercase "m" represents the serial number of ports (n=5, 6), and a lowercase "x" represents the serial number of the bits (x=0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 GPIO registers

Name	Address	Description	Reset value
P0	80h	P0 port input and output register	FFh
P0_DIR_PU	C5h	P0 port direction control and pull-up enable register	FFh
P0_MOD_OC	C4h	P0 port output mode register	FFh
P1	90h	P1 port input and output register	FFh
P1_DIR_PU	93h	P1 port direction control and pull-up enable register	FFh
P1_MOD_OC	92h	P1 port output mode register	FFh
P2	A0h	P2 port input and output register	FFh
P2_DIR_PU	95h	P2 port direction control and pull-up enable register	FFh
P2_MOD_OC	94h	P2 port output mode register	FFh
P3	B0h	P3 port input and output register	FFh
P3_DIR_PU	97h	P3 port direction control and pull-up enable register	FFh
P3_MOD_OC	96h	P3 port output mode register	FFh
P4	C0h	P4 port input and output register	FFh
P4_DIR_PU	C3h	P4 port direction control and pull-up enable register	FFh
P4_MOD_OC	C2h	P4 port output mode register	FFh
P4_LED_KEY	C1h	P4 port LED current limiting and keyboard mode register	00h
P5_IN	AAh	P5 port input register	PPh
P5_OUT_PU	ABh	P5 port output data and pull-up enable register	00h
P5_DIR	ACh	P5 port direction control register	00h

P6_IN	ADh	P6 port input register	PPh
P6_OUT_PU	AEh	P6 port output data and pull-up enable register	00h
P6_DIR	AFh	P6 port direction control register	00h
P7	F1h	P7 port input and output register	P3h
XBUS_AUX	A2h	External bus auxiliary setting register	00h
PORT_CFG	21EAh	Port interrupt and wake-up configuration register	00h
PIN_FUNC	21E9h	Pin function selection register	00h
ANA_PIN	21E8h	Analog pin digital input disable register	00h

Pn port input and output register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0～Pn.7	RW	Pn.x pin state input and data output bit, addressed in bits	FFh

Pn port output mode register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0- push-pull output; 1- open-drain output	FFh

Pn port direction control and pull-up enable register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR_PU	RW	Pn.x pin direction control in push-pull output mode: 0- input; 1- output. Pn.x pin pull-up resistor enable control in open-drain output mode: 0- disable pull-up resistor; 1- enable pull-up resistor.	FFh

Pm port input register (Pm_IN):

Bit	Name	Access	Description	Reset value
[7:0]	Pm.0 ~ Pm.7	RW	Pm.x pin status input bit	PPh

Pm port output data and pull-up enable register (Pm_OUT_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pm_OUT_PU	RW	Pm.x pin output data when Pm_DIR[x]=1: 0- output low level; 1- output high level. Pm.x pin pull-up resistor enable control when Pm_DIR[x]=0: 0- disable pull-up resistor; 1- enable pull-up resistor;	00h

Pm port direction control register (Pm_DIR):

Bit	Name	Access	Description	Reset value
[7:0]	Pm_DIR	RW	Pm.x pin direction control: 0- input; 1- output	00h

Relevant configuration of Pn port is implemented by the combination of Pn_MOD_OC[x] and Pn_DIR_PU[x] as follows.

Table 10.2.2 Port configuration register combination

Pn_MOD_OC	Pn_DIR_PU	Working mode description (for example used in P4.x only when P4_LED_KEY[x]=0)
0	0	High impedance input mode, pin has no pull-up or pull-down resistor
0	1	Push-pull output mode, with symmetrical drive capability, can output or absorb large current
1	0	Open-drain output, support high impedance input, pin has no pull-up resistor
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, support input, pin has pull-up resistor, when output is changed from low level to high level, it will automatically drive the high level of 2 clock cycles to accelerate the conversion

Table 10.2.3 Configuration register combination when P4.x port and P4_LED_KEY[x]=1

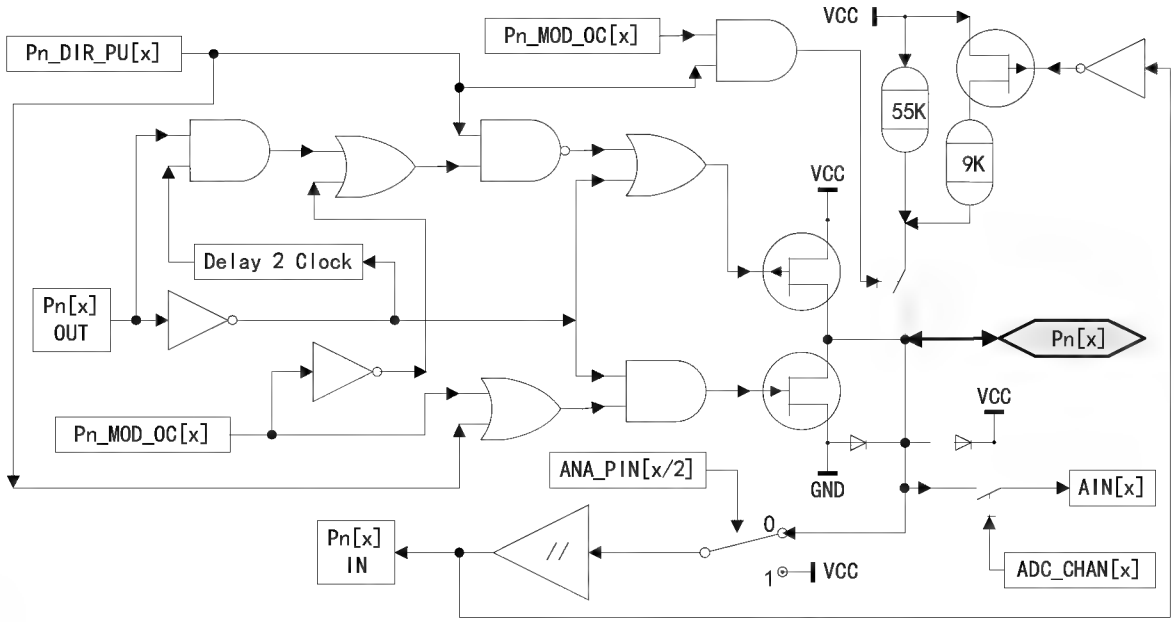
P4_MOD_OC	P4_DIR_PU	Working mode description (when P4_LED_KEY[x]=1)
0	0	High impedance input mode, pin has no pull-up or pull-down resistor
0	1	Push-pull output mode, it can output large current and absorb the limiting current to directly drive the LED
1	0	Open-drain output, support current-type keypad signal input, pin has no pull-up resistor
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, support current-type keypad signal input, pin has pull-up resistor, when output is changed from low level to high level, it will automatically drive the high level of 2 clock cycles to accelerate the conversion

Note: The current-type keyboard signal has built-in hardware to eliminate interference. After the key is pressed, the software needs to delay at least 500nS before sampling P4.

The P1～P4 ports support pure input or push-pull output and quasi-bidirectional modes, etc. Each pin has a freely controlled internal pull-up resistor, and a protective diode connected to VDD and GND.

Figure10.2.1 shows the equivalent schematic of the P0.x pin of the P0 port and the P1.x pin of the P1 port. After AIN, ADC_PIN and ADC_CHAN are removed, it can be applied to P2, P3 and P4.

Figure 10.2.1 I/O pin equivalent schematic



The resistance value in the figure is for reference only. For P0.0 ~ P0.7, P3.3 and P3.4, the 55K and 9K in the figure should be 5K and 60K respectively.

Table 10.2.4 Port P5.x configuration register combination

P5_DIR	P5_OUT_PU	Working mode description
0	0	High impedance input mode, pin has no pull-up or pull-down resistor
0	1	Input mode, pin has 7.5K pull-up resistor to VDD
1	0	Push-pull output mode, output low level, and absorb large current
1	1	Push-pull output mode, output high level, and output large current

Table 10.2.5 Port P6.x configuration register combination

P6_DIR	P6_OUT_PU	bUX_DP_PU_EN	Working mode description
0	0	0	High impedance input mode, pin has 1000K pull-down resistor
0	0	1	Input mode, pin has 1.5K pull-up resistor to V33.
0	1	0	Input mode, pin has 7.5K pull-up resistor to VDD. If enter power-down deep sleep mode when VDD is higher than 4V and USB is enabled, the 1.5K pull-up must be replaced by the 7.5K pull-up during sleep. Enable 7.5K and then disable 1.5K before sleep. Enable 1.5K and then disable 7.5K after wake-up.
1	0		Push-pull output mode, output low level, and absorb large current
1	1		Push-pull output mode, output high level, and output large current

P7 port input and output register (P7):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Reserved	00b
5	bP7_1_IN	RO	P7.1 pin data input bit	P
4	bP7_0_IN	RO	P7.0 pin data input bit	P
3	bP7_1_DIR	RW	P7.1 pin direction control: 0- input; 1- output	0
2	bP7_0_DIR	RW	P7.0 pin direction control: 0- input; 1- output	0
1	bP7_1_OUT_PU	RW	P7.1 pin output data when bP7_1_DIR =1: 0- output low level; 1- output high level. P7.1 pin pull-up resistor enable control when bP7_1_DIR =0: 0- disable pull-up resistor; 1- enable pull-up resistor;	1
0	bP7_0_OUT_PU	RW	P7.0 pin output data when bP7_0_DIR =1: 0- output low level; 1- output high level. P7.0 pin pull-up resistor enable control when bP7_0_DIR =0: 0- disable pull-up resistor; 1- enable pull-up resistor;	1

Table 10.2.6 Port P7.x configuration register combination

bP7_?_DIR	bP7_?_OUT_PU	bOSC_EN_XT	Working mode description
0	0	0	High impedance input mode, pin has no pull-up or pull-down resistor
0	1	0	Input mode, pin has pull-up resistor
1	0	0	Push-pull output mode, output low level, and absorb large current
1	1	0	Push-pull output mode, output high level, and output large current
X	X	1	P7.0/P7.1 is used as XI/XO for external crystal oscillator

Port interrupt and wake-up configuration register (PORT_CFG):

Bit	Name	Access	Description	Reset value
7	bP4_IE_LEVEL	RW	Interrupt enable and wake-up enable of any pin level change from P4.0 to P4.7: 0- Interrupt and wakeup disabled; 1- Interrupt and wakeup enabled.	0
6	bP2L_IE_LEVEL	RW	Interrupt enable and wake-up enable of any pin level change from P2.0 to P2.3: 0- Interrupt and wakeup disabled; 1- Interrupt and wakeup enabled.	0
5	bP1L_IE_LEVEL	RW	Interrupt enable and wake-up enable of any pin level change from P1.0 to P1.3: 0- Interrupt and wakeup disabled;	0

			1- Interrupt and wakeup enabled.	
4	bP0_IE_LEVEL	RW	Interrupt enable and wake-up enable of any pin level change from P0.0 to P0.7: 0- Interrupt and wakeup disabled; 1- Interrupt and wakeup enabled.	0
[3:0]	Reserved	RO	Reserved	0000b

Analog pin digital input disable register (ANA_PIN):

Bit	Name	Access	Description	Reset value
7	bP70_P71_DI_DIS	RW	Control P7.0 and P7.1 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0
6	bAIN12_13_DI_DIS	RW	Control AIN12 and AIN13 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0
5	bAIN10_11_DI_DIS	RW	Control AIN10 and AIN11 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0
4	bAIN8_9_DI_DIS	RW	Control AIN8 and AIN9 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0
3	bAIN6_7_DI_DIS	RW	Control AIN6 and AIN7 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0
2	bAIN4_5_DI_DIS	RW	Control AIN4 and AIN5 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0
1	bAIN2_3_DI_DIS	RW	Control AIN2 and AIN3 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0
0	bAIN0_1_DI_DIS	RW	Control AIN0 and AIN1 digital input: 0- Digital input enabled; 1- Digital input disabled, to save power consumption	0

10.3 GPIO alternate functions and map

Some I/O pins of CH555 have alternate functions. After power on, they are all general-purpose I/O pins by default. After enabling different function modules, the corresponding pins are configured as corresponding function pins of each function module.

Pin function selection register (PIN_FUNC):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0

5	bUART1_PIN_X	RW	UART1 pin mapping enable bit 0: RXD1/TXD1 selects P2.6/P2.7. 1: RXD1/TXD1 selects P1.6/P1.7	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable bit 0: RXD0/TXD0 selects P3.0/P3.1. 1: RXD0/TXD0 selects P0.2/P0.3	0
3	bIO_INT_ACT	RO	GPIO interrupt request activation status: When bIE_IO_EDGE=0, 1: GPIO inputs valid level and requests interrupt. 0: Input level is invalid. When bIE_IO_EDGE=1, the bit is used as the edge interrupt flag, 1: Valid edge is detected and the bit cannot be cleared by software and can only be cleared automatically when reset or in level interrupt mode or when enterring the corresponding interrupt service program.	0
2	bINT0_PIN_X	RW	INT0 pin mapping enable bit 0: INT0 selects P3.2. 1: INT0 selects P1.2.	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable bit 0: T2EX/CAP2 selects P1.1. 1: T2EX/CAP2 selects P2.5.	0
0	bT2_PIN_X	RW	T2/CAP1 pin mapping enable bit 0: T2/CAP1 selects P1.0. 1: T2/CAP1 selects P2.4	0

Table 10.3.1 Alternate functions of GPIO pins

GPIO	Other functions: priority sequence from left to right
P0[0]	SCL0/bSCL0, AIN8, P0.0
P0[1]	SDA0/bSDA0, AIN9, P0.1
P0[2]	RXD_/bRXD_, AIN10, P0.2
P0[3]	TXD_/bTXD_, AIN11, P0.3
P0[4]	AIN12, P0.4
P0[5]	AIN13, P0.5
P0[6]	P0.6
P0[7]	P0.7
P1[0]	T2/bT2, CAP1/bCAP1, AIN0, P1.0
P1[1]	T2EX/bT2EX, CAP2/bCAP2, AIN1, P1.1
P1[2]	INT0_/bINT0, AIN2, P1.2
P1[3]	AIN3, P1.3
P1[4]	SCS/bSCS, AIN4, P1.4
P1[5]	MOSI/bMOSI, AIN5, P1.5
P1[6]	MISO/bMISO, RXD1_/bRXD1_, AIN6, P1.6
P1[7]	SCK/bSCK, TXD1_/bTXD1_, AIN7, P1.7

P2[0]～P2[3]	P2.0～P2.3
P2[4]	T2_/bT2_, CAP1_/bCAP1_, P2.4
P2[5]	T2EX_/bT2EX_, CAP2_/bCAP2_, P2.5
P2[6]	RXD1/bRXD1, P2.6
P2[7]	TXD1/bTXD1, P2.7
P3[0]	RXD/bRXD, P3.0
P3[1]	TXD/bTXD, P3.1
P3[2]	INT0/bINT0, P3.2
P3[3]	INT1/bINT1, P3.3
P3[4]	T0/bT0, P3.4
P3[5]	MOSI1/bMOSI1, T1/bT1, P3.5
P3[6]	MISO1/bMISO1, P3.6
P3[7]	SCK1/bSCK1, P3.7
P4[0]～P4[7]	P4.0～P4.7
P5[0]～P5[7]	P5.0～P5.7
P6[0]	bDM, P6.0
P6[1]	bDP, P6.1
P6[2]	P6.2
P6[3]	P6.3
P6[4]	bDCO_, P6.4
P6[5]	P6.5
P6[6]	P6.6
P6[7]	P6.7
P7[0]	XI, P7.0
P7[1]	XO, bRST, bALE, P7.1

The priority sequence from left to right mentioned in the above table refers to the priority when multiple function modules compete to use the GPIO.

11. External bus (xBUS)

CH555 does not provide bus signals for the outside, and it does not support the external bus, but can normally access the on-chip xRAM.

External bus auxiliary setting register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	RO	UART0 transmit status 1: Transmission is in progress.	0
6	bUART0_RX	RO	UART0 receive status 1: Reception is in progress.	0
5	bSAFE_MOD_ACT	RO	Safe mode status 1: In safe mode currently.	0
4	bALE_CLK_EN	RW	ALE pin clock output enable 1: P7.1 selected to output the divided clock of system clock frequency (when P5_DIR[2]=0 and	0

			bP7_1_DIR=1 and bOSC_EN_XT=0). 0: Output clock signal disabled.	
3	bALE_CLK_SEL	RW	ALE pin clock frequency selection when bALE_CLK_EN=1; 0: Divided by 12. 1: Divided by 4.	0
3	GF2	RW	General flag bit 2 when bALE_CLK_EN=0: User-defined. Cleared and set by software.	0
2	bDPTR_AUTO_INC	RW	Enable DPTR to add 1 automatically after the completion of MOVX_@DPTR command	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Dual DPTR data pointers selection bit: 0: DPTR0 selected. 1: DPTR1 selected	0

Table 11.1 P7.1 pin alternate ALE output state table

bALE_CLK_EN	bALE_CLK_SEL	bP7_1_OUT_PU@P7.1	P7.1 selected pin function description
0	X	X	Default status, disable ALE
1	0	0	Output Fsys/12
1	1	0	Output Fsys/4
X	X	1	Output high level

12. Timer

12.1 Timer0/1

Timer0 and Timer1 are 2 16-bit timers/counters, configured by TCON and TMOD. TCON is used for startup control and overflow interrupt as well as external interrupt control of timer/counter T0 and T1. Each timer is a 16-bit timing unit composed of dual 8-bit registers. The high byte counter of Timer0 is TH0 and the low byte is TL0. The high byte counter of Timer1 is TH1 and the low byte is TL1. Timer1 can also be used as the baud rate generator of UART0.

Table 12.1.1 Timer0/1 related registers

Name	Address	Description	Reset value
TH1	8Dh	Timer1 count high byte	xxh
TH0	8Ch	Timer0 count high byte	xxh
TL1	8Bh	Timer1 count low byte	xxh
TL0	8Ah	Timer0 count low byte	xxh
TMOD	89h	Timer0/1 mode register	00h
TCON	88h	Timer0/1 control register	00h

Timer/counter 0/1 control register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag bit. Automatically cleared after entering Timer1 interrupt	0

6	TR1	RW	Timer1 startup/stop bit. Set 1 to start. Set and cleared by software	0
5	TF0	RW	Timer0 overflow interrupt flag bit. Automatically cleared after entering Timer0 interrupt	0
4	TR0	RW	Timer0 startup/stop bit. Set 1 to start. Set and cleared by software	0
3	IE1	RW	Interrupt request flag bit of INT1 external interrupt 1. Automatically cleared after entering interrupt	0
2	IT1	RW	Trigger mode control bit of INT1 external interrupt 1. 0: Low level trigger selected for external interrupt. 1: Falling edge trigger selected for external interrupt	0
1	IE0	RW	INT0 interrupt request flag bit Automatically cleared after entering interrupt	0
0	IT0	RW	INT0 trigger mode control bit 0: Low level trigger selected for external interrupt; 1: Falling trigger selected for external interrupt	0

Timer/counter 0/1 mode register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Gate control enable bit, controls whether Timer1 startup is affected by the external interrupt signal INT1. 0: Whether the timer/counter 1 starts is not related to INT1. 1: Only start when INT1 pin is at high level and TR1 is 1	0
6	bT1_CT	RW	Timing or counting mode selection bit 0: Timing mode. 1: Counting mode. Falling edge of T1 pin selected as clock.	0
5	bT1_M1	RW	Timer/counter1 mode selection high bit	0
4	bT1_M0	RW	Timer/counter1 mode selection low bit	0
3	bT0_GATE	RW	Gate control enable bit, controls whether Timer0 startup is affected by the external interrupt signal INT0. 0: Whether the timer/counter 0 starts is not related to INT0. 1: Only start when INT0 pin is at high level and TR0 is 1.	0
2	bT0_CT	RW	Timing or counting mode selection bit 0: Timing mode. 1: Counting mode. Falling edge of T0 pin selected as clock	0
1	bT0_M1	RW	Timer/counter 0 mode selection high bit	0
0	bT0_M0	RW	Timer/counter 0 mode selection low bit	0

Table 12.1.2 Timern working mode selection by configuring bTn_M1 and bTn_M0 (n=0, 1)

bTn_M1	bTn_M0	Timern working mode (n=0,1)
0	0	Mode 0: 13-bit timer/counter n, the counting unit is composed of the lower 5 bits of TLn and THn, and the higher 3 bits of TLn are invalid. When counts of all 13 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
0	1	Mode 1: 16-bit timer/counter n, the counting unit is composed of TLn and THn. When counts of all 16 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
1	0	Mode 2: 8-bit reload timer/counter n, TLn is used as the counting unit, and THn is used as the reload counting unit. When counts of all 8 bits change from 1 to 0, set the overflow flag TFn and automatically load the initial value from THn.
1	1	Mode 3: If it is timer/counter0, then timer/counter0 is divided into 2 parts, TL0 and TH0. TL0 is used as 8-bit timer/counter, occupying all control bits of Timer0. TH0 is also used as another 8-bit timer, occupying TR1, TF1 and interrupt resources of Timer1. At this time, Timer1 is still available, but the startup control bit TR1 and overflow flag bit TF1 cannot be used. If it is timer/counter1, it will stop when enterring mode 3.

Timern count low byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	xxh

Timern count high byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	xxh

12.2 Timer2

Timer2 is a 16-bit automatic reload timer/counter, configured by T2CON and T2MOD registers, with TH2 as the high byte counter of Timer2 and TL2 as the low byte counter. Timer2 can be used as the baud rate generator of UART0, and it has the function of 2-channel signal level capture. The capture count is stored in RCAP2 and T2CAP1 registers.

Table 12.2.1 Timer2 related registers

Name	Address	Description	Reset value
TH2	CDh	Timer2 counter high byte	00h
TL2	CCh	Timer2 counter low byte	00h
T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxh
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxh
T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	xxxxh
RCAP2H	CBh	Count reload/capature 2 data register high byte	00h
RCAP2L	CAh	Count reload/capature 2 data register low byte	00h
RCAP2	CAh	RCAP2L and RCAP2H constitute a 16-bit SFR	0000h
T2MOD	C9h	Timer2 mode register	00h

T2CON	C8h	Timer2 control register	00h

Timer/counter 2 control register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	Timer2 overflow interrupt flag when bT2_CAP1_EN=0, when Timer2 count of all 16 bits changes from 1 to 0, set the overflow flag as 1, which requires software to clear. When RCLK=1 or TCLK=1, the bit is not set to 1.	0
7	CAP1F	RW	Timer2 capture 1 interrupt flag when bT2_CAP1_EN=1, triggered by the valid edge of T2, which requires software to clear it	0
6	EXF2	RW	Timer2 external trigger flag, when EXEN2=1, triggered and set as 1 by T2EX valid edge, which requires software to clear.	0
5	RCLK	RW	UART0 receiving clock selection 0: Timer1 overflow pulse selected to generate the baud rate. 1: Timer2 overflow pulse selected to generate the baud rate	0
4	TCLK	RW	UART0 tranmit clock selection 0: Timer1 overflow pulse selected to generate baud rate. 1: Timer2 overflow pulse selected to generate the baud rate	0
3	EXEN2	RW	T2EX trigger enable bit 0: Ignore T2EX. 1: Enable reload or capture triggered in T2EX valid edge	0
2	TR2	RW	Timer2 startup/stop bit Set 1 to start. Set and cleared by software	0
1	C_T2	RW	Timer2 clock source selection bit. 0: Internal clock selected. 1: Edge count based on T2 pin falling edge selected	0
0	CP_RL2	RW	Timer2 function selection bit, should be forced to be 0 if RCLK or TCLK is 1. 0: Timer2 selected as timer/counter, to automatically reload the initial value of the count when the counter overflows or T2EX level changes. 1: Timer2 capture 2 function enabled, and the valid edge of T2EX captured	0

Timer/counter 2 mode register (T2MOD):

Bit	Name	Access	Description	Reset value
7	bTMR_CLK	RW	The fastest clock mode enable of T0/T1/T2 timer that has selected fast clock 1: System clock frequency whithout division (Fsys) selected as the count clock. 0: Divided clock selected. This bit has no effect on the timer that selects the	0

			standard clock.		
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit 0: Standard clock, Fsys/12 in timing/counting mode, and Fsys/4 in UART0 clock mode. 1: Fast clock, Fsys/4(bTMR_CLK=0) or Fsys(bTMR_CLK=1), and Fsys/2(bTMR_CLK=0) or Fsys (bTMR_CLK=1) in UART0 clock mode.		0
5	bT1_CLK	RW	Timer1 internal clock frequency selection bit 0: Standard clock, Fsys/12. 1: Fast clock Fsys/4(bTMR_CLK=0) or Fsys(bTMR_CLK=1)		0
4	bT0_CLK	RW	Timer0 internal clock frequency selection bit 0: Standard clock, Fsys/12. 1: Fast clock Fsys/4(bTMR_CLK=0) or Fsys(bTMR_CLK=1)		0
3	bT2_CAP_M1	RW	Timer2 capture mode high bit	Capture mode selection: X0: from falling edge to falling edge 01: from any edge to any edge, i.e. level change 11: from rising edge to rising edge	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit		0
1	T2OE	RW	Timer2 clock output enable bit 0: Output disabled. If the bit is 1: T2 pin output clock enabled, and the frequency is the half of the Timer2 overflow rate		0
0	bT2_CAP1_EN	RW	Capture 1 mode enable when RCLK=0, TCLK=0, CP_RL2=1, C_T2=0, T2OE=0 1: Capture 1 function enabled to capture valid edge of T2. 0: Capture 1 disabled.		0

Count reload/capature 2 data register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timer/counter mode; High byte of timer captured by CAP2 in capture mode	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timer/counter mode; Low byte of timer captured by CAP2 in capture mode	00h

Timer2 counter (T2COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (T2CAP1):

Bit	Name	Access	Description	Reset value
[7:0]	T2CAP1H	RO	High byte of timer captured by CAP1	xxh
[7:0]	T2CAP1L	RO	Low byte of timer captured by CAP1	xxh

12.3 Reserved

12.4 Reserved

12.5 Timer function

12.5.1 Timer0/1

(1). Set T2MOD, to select Timer internal clock frequency, if bTn_CLK(n=0/1) is 0, then the corresponding clock of Timer0/1 is Fsys/12. If bTn_CLK is 1, then select Fsys/4 or Fsys as the clock based on bTMR_CLK=0 or 1.

(2). Set TMOD to configure the working mode of Timer.

Mode 0: 13-bit timer/counter

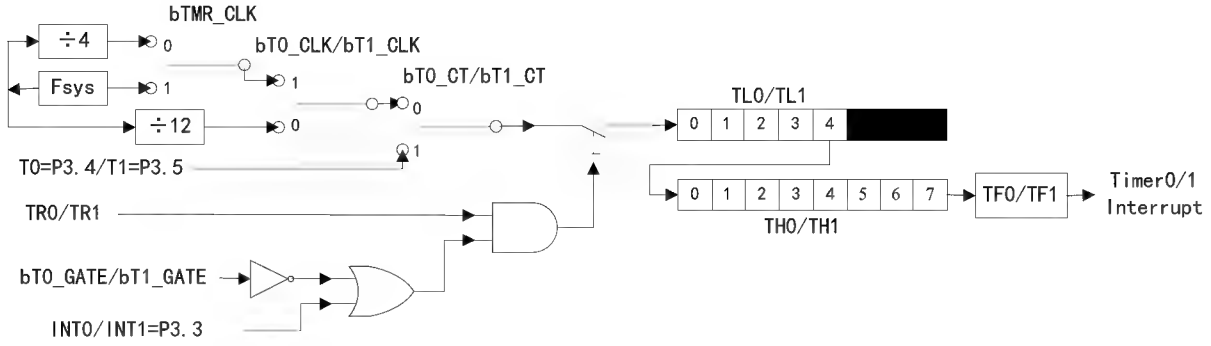


Figure 12.5.1.1 Timer0/1 mode 0

Mode 1: 16-bit timer/counter

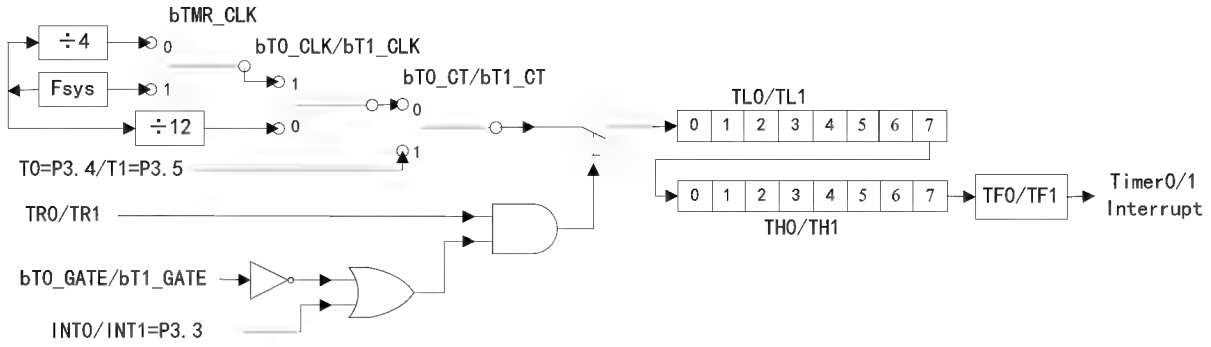


Figure 12.5.1.2 Timer0/1 mode 1

Mode 2: automatic reload 8-bit timer/counter

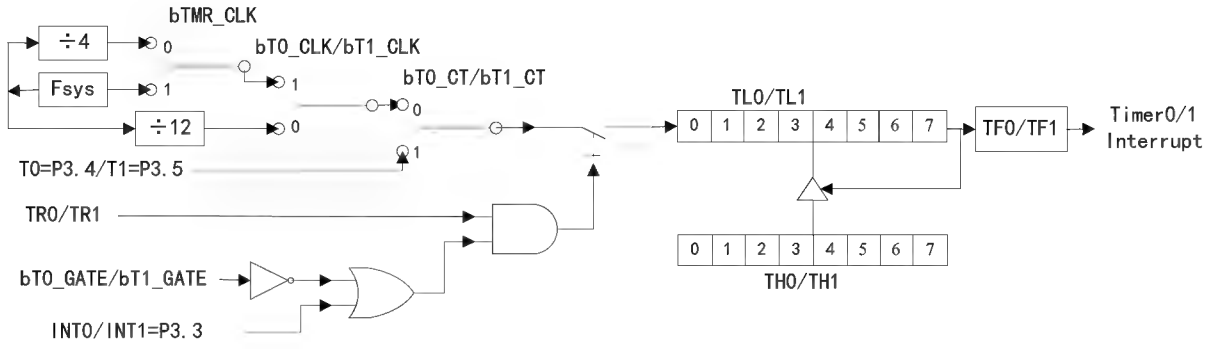


Figure12.5.1.3 Timer0/1 mode 2

Mode 3: Timer0 is divided into two independent 8-bit timers/counters and borrows the TR1 control bit of Timer1. Timer1 substitutes the borrowed TR1 control bit by whether starting mode 3, and stops running when it enters mode 3.

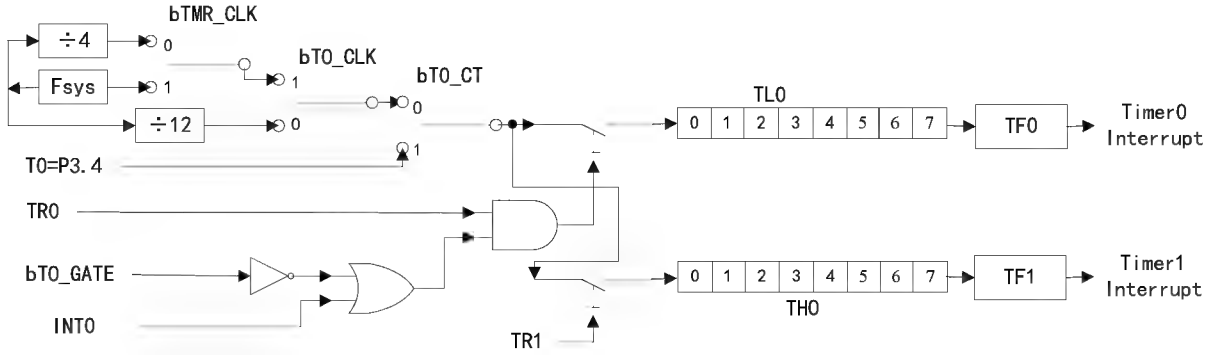


Figure 12.5.1.4 Timer0 mode 3

(3). Set initial value TLn and THn(n=0/1) of timer/counter.

(4). Set the TRn(n=0/1) bit in TCON to start or stop timer/counter, it can be checked by bit TFn(n=0/1) to query or by interrupt mode.

12.5.2 Timer2

Timer2 16-bit reload timer/counter mode:

(1). Set RCLK and TCLK in T2CON to 0, select non-UART baud rate generator mode.

(2). Set C_T2 in T2CON to 0, select to use internal clock, and turn to step (3); alternatively, set to 1 to select the falling edge of T2 pin as the count clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, then Timer2 clock is Fsys/12. If bT2_CLK is 1, then Fsys/4 or Fsys is selected as clock based on bTMR_CLK=0 or 1.

(4). Set CP_RL2 in T2CON to 0, and select 16-bit reload timer/counter function of Timer2.

(5). Set RCAP2L and RCAP2H as the reload value of timer after overflow, set TL2 and TH2 as the initial value of the timer (generally it is the same as RCAP2L and RCAP2H), set TR2 to 1 and turn on Timer2.

(6). Inquire TF2 or Timer2 interrupt to obtain the current timer/counter state.

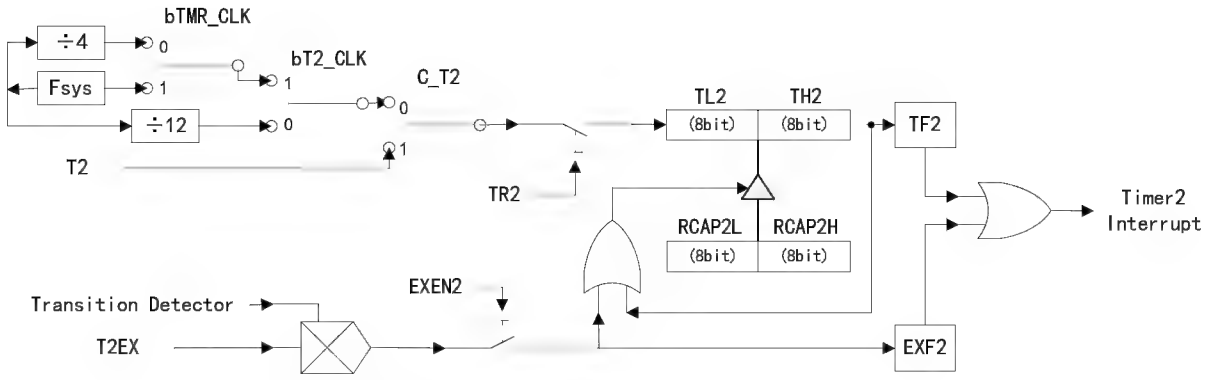


Figure 12.5.2.1 Timer2 16-bit reload timer/counter

Timer2 clock output mode:

Refer to the 16-bit reload timer/counter mode and then set the T2OE bit in T2MOD to 1 to enable a divided clock (TF2 frequency divided by 2) output from T2 pin.

Timer2 UART0 baud rate generator mode:

(1). Set the C_T2 bit in T2CON to 0, to select the internal clock. Alternatively, set to 1 to select the falling edge of T2 pin as the clock. Set RCLK and TCLK in T2CON to 1, or set one of them to 1 as required, to select UART baud rate generator mode.

(2). Set T2MOD, to select Timer internal clock frequency. If bT2_CLK is 0, then the clock of Timer2 is Fsys/4. If bT2_CLK is 1, then select Fsys/2 or Fsys as the clock based on bTMR_CLK=0 or 1.

(3). Set RCAP2L and RCAP2H as the reload value of timer after overflow, set TR2 to 1 to turn on Timer2.

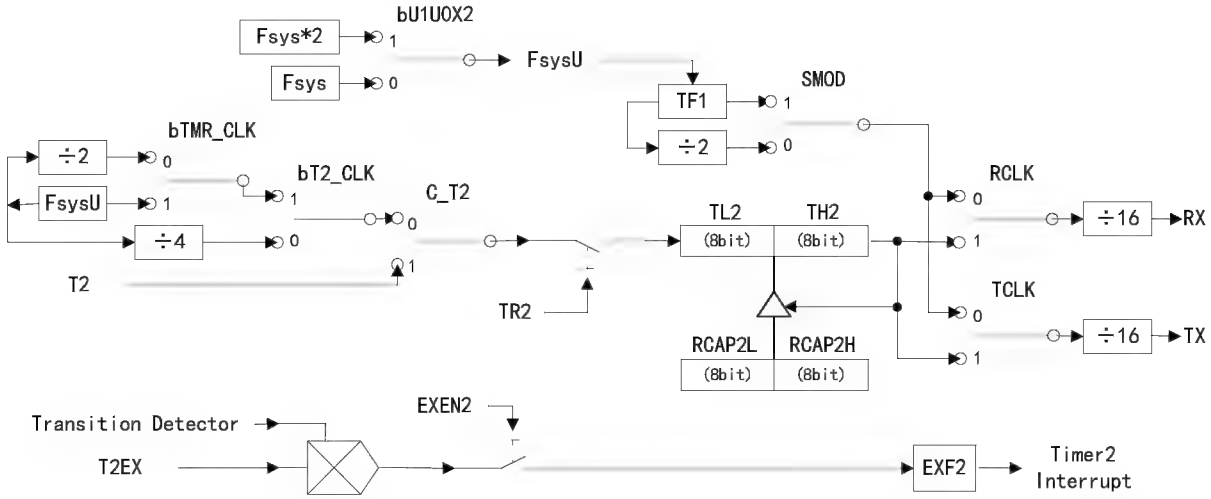


Figure 12.5.2.2 Timer2 UART0 baud rate generator

Timer2 signal channel capture mode:

(1). Set RCLK and TCLK in T2CON to 0, to select the non-UART baud rate generator mode.

(2). Set the C_T2 bit in T2CON to 0, to select the internal clock, and turn to step (3). Alternatively, set to 1 to select the falling edge of T2 pin as the counting clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, then Timer2 clock is Fsys/12. If bT2_CLK is 1, then Fsys/4 or Fsys is selected as the clock based on bTMR_CLK=0 or 1.

(4). Set bT2_CAP_M1 and bT2_CAP_M0 in T2MOD, to select corresponding edge capture mode.

(5). Set CP_RL2 in T2CON to 1, to select the capture function of Timer2 to T2EX pin.

(6). Set TL2 and TH2 as the initial value of the timer, and set TR2 to 1 and turn on Timer2.

(7). When CAP2 capture is completed, RCAP2L and RCAP2H will save the current count values of TL2 and TH2 and set EXF2 to generate interrupt. The difference value between the next captured RCAP2L and RCAP2H and the last captured RCAP2L and RCAP2H is the signal width between the two valid edges.

(8). If the C_T2 bit in T2CON is 0, and the bT2_CAP1_EN bit in T2MOD is 1, Timer2 will be enabled to capture the T2 pin at the same time. When the CAP1 capture is completed, T2CAP1L and T2CAP1H will save the current count values of TL2 and TH2, and set CAP1F to generate interrupt.

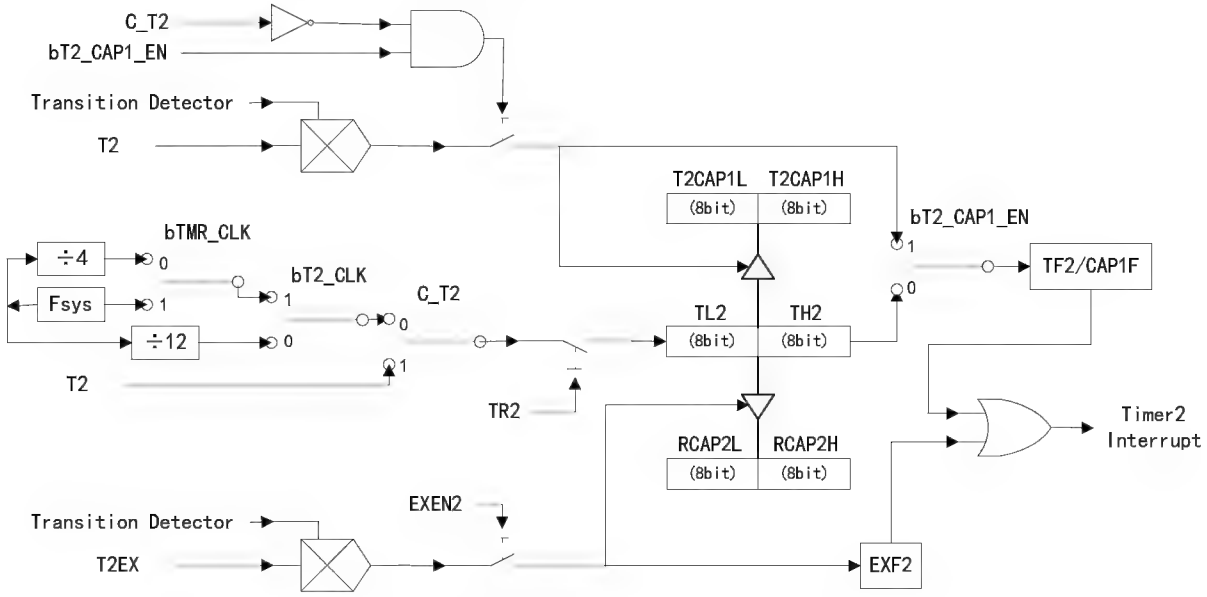


Figure 12.5.2.3 Timer2 capture mode

13. Universal asynchronous receiver transmitter (UART)

13.1 UART introduction

CH555 provides 2 full-duplex UARTs: UART0 and UART1.

UART0 is a standard MCS51 serial port, whose data reception/transmission is implemented by physically separated receive/transmit registers via SBUF access. The data written to SBUF is loaded into the transmit register, and the read operation to SBUF corresponds to the receive buffer register.

UART1 is a simplified MCS51 serial port, whose data reception/transmission is implemented by physically separated receive/transmit registers via SBUF access. The data written to SBUF1 is loaded into the transmit register, and the read operation to SBUF1 corresponds to the receive buffer register. Compared with UART0, UART1 has removed the multi-device communication mode and fixed baud rate, and UART1 has independent baud rate generator.

13.2 UART register

Table 13.2.1 UART related registers

Name	Address	Description	Reset value
SBUF	99h	UART0 data register	xxh
SCON	98h	UART0 control register	00h
SCON1	BCh	UART1 control register	00h

SBUF1	BDh	UART1 data register	xxh
SBAUD1	BEh	UART1 baud rate setting register	xxh
SIF1	BFh	UART1 interrupt status register	00h

13.2.1 UART0 register description

UART0 control register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 working mode selection bit 0 0: 8-bit data asynchronous communication. 1: 9-bit data asynchronous communication.	0
6	SM1	RW	UART0 working mode selection bit 1 0, set fixed baud rate. If the bit is 1, set variable baud rate, generated by timer T1 or T2.	0
5	SM2	RW	UART0 multi-device communication control bit: When receiving data in mode2 or mode3, and SM2=1, if RB8 is 0, then RI is not set to 1 and the receiving is invalid. If RB8 is 1, then RI is set to 1 and the receiving is valid. When SM2=0, no matter RB8 is 0 or 1, RI is set when receiving data and the receiving is valid. In mode1, if SM2=1, only when the valid stop bit is received can the reception be valid. In mode 0, the bit SM2 must be set to 0.	0
4	REN	RW	UART0 receive enable bit 0: Receive disabled. 1: Receive enabled.	0
3	TB8	RW	The 9th bit of the transmitted data, in mode2 and mode3, TB8 is used to write the 9th bit of the transmitted data, which can be a parity bit. In multi-device communication, it is used to indicate whether the host transmits an address byte or a data byte. Data byte when TB8=0. Address byte when TB8=1.	0
2	RB8	RW	The 9th bit of the received data, in mode2 and mode3, RB8 is used to store the 9th bit of the received data. In mode1, if SM2=0, then RB8 is used to store the received stop bit. In mode0, RB8 is not used.	0
1	TI	RW	Transmit interrupt flag bit. Set by hardware after a data byte is sent. Cleared by software.	0
0	RI	RW	Receiving interrupt flag bit. Set by hardware after a data byte is received effectively. Cleared by software.	0

Table 13.2.1.1 UART0 working mode selection

SM0	SM1	Description
0	0	Mode 0, shift register mode, baud rate is fixed to be Fsys/12
0	1	Mode 1, 8-bit asynchronous communication mode, variable baud rate, generated by timer T1 or T2

1	0	Mode 2, 9-bit asynchronous communication mode, baud rate is Fsys/128(SMOD=0) or Fsys/32(SMOD=1)
1	1	Mode 3, 9-bit asynchronous communication mode, variable baud rate, generated by timer T1 or T2

In mode1 and mode3, when RCLK=0 and TCLK=0, UART0 baud rate is generated by timer T1. T1 should be set in mode 2 automatic reload 8-bit timer mode, both bT1_CT and bT1_GATE must be 0. There are the following clock types.

Table 13.2.1.2 Calculation of UART0 baud rate generated by T1

bTMR_CLK	bT1_CLK	SMOD	Description (When bU1U0X2=1, the baud rate doubles)
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In mode1 and mode3, when RCLK=1 or TCLK=1, UART0 baud rate is generated by timer T2. T2 should be set in 16-bit automatic reload baud rate generator mode, both C_T2 and CP_RL2 must be 0. There are the following clock types.

Table 13.2.1.3 Calculation formula of UART0 baud rate generated by T2

bTMR_CLK	bT2_CLK	Description (When bU1U0X2=1, the baud rate doubles)
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 data register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF. The receive register is used to read data from SBUF.	xxh

13.2.2 UART1 register description

UART1 control register (SCON1):

Bit	Name	Access	Description	Reset value
7	bU1SM0	RW	UART1 working mode selection bit 0: 8-bit data asynchronous communication. 1: 9-bit data asynchronous communication.	0
6	bU1U0X2	RW	UART1/UART0 clock multiplier enable: 0: Disabled. The clock frequency is Fsys; 1: Enabled. The clock frequency is 2*Fsys, all communication baud rates of UART1 and UART0 are	0

			doubled.	
5	bU1SMOD	RW	UART1 communication baud rate selection: 0: Slow mode; 1: Fast mode	0
4	bU1REN	RW	UART1 receive enable bit 0: Receive disabled. 1: Receive enabled.	0
3	bU1TB8	RW	The 9th bit of the transmitted data, in 9-bit data mode, TB8 is used to write the 9th bit of the transmitted data, which can be a parity bit. In 8-bit data mode, TB8 is ignored	0
2	bU1RB8	RW	The 9th bit of the received data, in 9-bit data mode, RB8 is used to store the 9th bit of the received data. In 8-bit data mode, RB8 is used to store the received stop bit	0
1	bU1TIS	WO	Write 1 to preset the transmit interrupt flag bit as 1, and the read operation always returns 0.	0
0	bU1RIS	WO	Write 1 to preset the receiving interrupt flag bit as 1, and the read operation always returns 0.	0

UART1 baud rate is generated by SBAUD1 setting and can be divided into several cases according to the selection of bU1SMOD:

When bU1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate;

When bU1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

When bU1U0X2=1, the above baud rate doubles.

UART1 interrupt status register (SIF1):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU1TI	RW	Transmit interrupt flag bit. Set by hardware after a data byte is sent, requires software to write 1 to clear (0 written to such bit will be ignored)	0
0	bU1RI	RW	Receive interrupt flag bit. Set by hardware after a data byte is received effectively, requires software to write 1 to clear (write 0 to such bit will be ignored)	0

Notes: Write 1 to the interrupt flag bit to clear, and this ensures that only the specified flag bit is cleared without affecting other interrupt flags in the same register (other interrupt flags may have been 1 before the write operation or may become 1 during the write operation). Similarly hereinafter.

UART1 data register (SBUF1):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF1	RW	UART1 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF1. The receive register is used to read data from SBUF1.	xxh

13.3 UART applications

UART0 application:

(1). Select UART0 baud rate generator, either from T1 or T2, and configure corresponding counter.

(2). Turn on the timer T1 or T2.

(3).Set SM0, SM1, SM2 in SCON to select the working mode of UART0. Set REN as 1 to enable UART0 receiving.

(4). UART interrupt can be set or R1 and T1 interrupt state can be inquired.

(5). Read and write SBUF to implement data reception and transmission of UART, and the allowable baud rate error of the UART receive signal is not more than 2%.

UART1 application:

(1). Select bU1SMOD and set SBAUD1 based on the baud rate.

(2).Set bU1SM0 in SCON1 to select the working mode of UART1. Set bU1REN as 1 and enable UART1 receiving.

(3). UART1 interrupt can be set or bU1RI and bU1TI interrupt state can be inquired (only write 1 to the specified bit to reset).

(4). Read/write SBUF1 to implement data reception and transmission of UART1, and the allowable baud rate error of UART receive signal is not more than 2%.

14. Serial peripheral interface (SPI)

14.1 SPI introduction

CH555 provides 2 SPIs, for high-speed synchronous data transmission with peripherals.

Features of SPI0:

(1). Support master mode and slave mode;

(2). Support mode 0 and mode 3 clock mode;

(3). Optional, 3-line full duplex or 2-line half-duplex mode;

(4). Optional, MSB sent first or LSB sent first;

(5). Clock frequency is adjustable, up to half of the system clock frequency;

(6). Built-in 1 byte receiver FIFO and 1 byte transmitter FIFO;

(7). Support the first byte pre-load data in slave mode to facilitate the host to obtain the returned data immediately in the first byte.

Features of SPI1:

(1). Support only master mode, MSB sent first;

(2). Support mode 0 and mode 3 clock mode;

(3). Optional, 3-line full duplex or 2-line half-duplex mode;

(4). Clock frequency is adjustable, up to half of the system clock frequency.

14.2 SPI register

Table 14.2.1 SPI related registers

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 setting register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock setting register	20h

SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 receive/transmit data register	xxh
SPI0_STAT	F8h	SPI0 status register	08h
SPI1_CK_SE	B7h	SPI1 clock setting register	20h
SPI1_CTRL	B6h	SPI1 control register	02h
SPI1_DATA	B5h	SPI1 receive/transmit data register	xxh
SPI1_STAT	B4h	SPI1 status register	08h

14.2.1 SPI0 register description

SPI0 setting register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master/slave mode selection bit 0: SPI0 is in master mode. 1: SPI0 is in slave mode/device mode.	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable bit in slave mode. 1: FIFO overflow interrupt enabled. 0: FIFO overflow interrupt disabled.	0
5	bS0_IE_FIRST	RW	Receive first byte complete interrupt enable bit in slave mode 1: Interrupt triggerred when the first data byte is received in slave mode. 0: Interrupt is not generated when the first byte is received.	0
4	bS0_IE_BYTE	RW	Data byte transfer complete interrupt enable bit. 1: Byte transfer complete interrupt enabled. 0: Byte transfer complete interrupt disabled.	0
3	bS0_BIT_ORDER	RW	Order control bit of data byte 0: MSB first. 1: LSB first.	0
2	Reserved	RO	Reserved	0
1	bS0_SLV_SELT	RO	Chip select activation status bit in slave mode. 0: Not selected currently. 1: Being selected currently.	0
0	bS0_SLV_PRELOAD	RO	Preload data status bit in slave mode 1: Currently in pre-load state after Chip Select is valid and before data is transferred.	0

SPI0 clock setting register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	Set SPI0 clock frequency division factor in master mode	20h

SPI0 preset data register in slave mode (SPI0_S_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Preload first transmitted data in slave mode	20h

SPI0 control register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	MISO output enable bit of SPI0 1: Enabled. 0: Disabled.	0
6	bS0_MOSI_OE	RW	MOSI output enable bit of SPI0 1: Enabled. 0: Disabled.	0
5	bS0_SCK_OE	RW	SCK output enable bit of SPI0 1: Enabled. 0: Disabled.	0
4	bS0_DATA_DIR	RW	SPI0 data direction control bit 0: Output. Only write FIFO operation is regarded as valid, and start one SPI transmission. 1: Input. Write/read FIFO operation is regarded as valid, and start one SPI transmission.	0
3	bS0_MST_CLK	RW	SPI0 host clock mode control bit 0: Mode 0. SCK is at low level by default when idle. 1: Mode 3. SCK is at high level by default.	0
2	bS0_2_WIRE	RW	2-wire half-duplex mode enable bit of SPI0 0: 3-wire full-duplex mode (SCK, MOSI and MISO). 1: 2-wire half-duplex mode (SCK, MISO).	0
1	bS0_CLR_ALL	RW	1: Empty SPI0 interrupt flag and FIFO. Cleared by software.	1
0	bS0_AUTO_IF	RW	Byte receive done interrupt flag auto reset enable bit through FIFO valid operation 1: Automatically reset the byte receive done interrupt flag (S0_IF_BYTE) during valid read/write operation of FIFO	0

SPI0 receive/transmit data register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Including the transmit FIFO and the receive FIFO that are physically separated. The receive FIFO is used for read operation. The transmit FIFO is used for write operation. Valid read/write operation can start one SPI transmission.	xxh

SPI0 status register (SPI0_STAT):

Bit	Name	Access	Description	Reset value
7	S0_FST_ACT	RO	1: The first byte reception is completed in slave mode	0
6	S0_IF_OV	RW	FIFO overflow flag bit in slave mode 1: FIFO overflow interrupt. 0: No interrupt.	0

			Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. When bS0_DATA_DIR=0, transmit FIFO empty triggers interrupt. When bS0_DATA_DIR=1, receive FIFO full triggers interrupt.	
5	S0_IF_FIRST	RW	First byte reception done interrupt flag bit in slave mode 1: The first byte is received. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	S0_IF_BYTE	RW	Data byte transmission done interrupt flag bit 1: One byte transmission is done. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset, or reset by FIFO valid operation when bS0_AUTO_IF=1	0
3	S0_FREE	RO	SPI0 free flag bit 1: No SPI shift at present, usually it is in free period between data bytes	1
2	S0_T_FIFO	RO	SPI0 transmit FIFO count. The valid value is 0 or 1.	0
1	Reserved	RO	Reserved	0
0	S0_R_FIFO	RO	SPI0 receive FIFO count. The valid value is 0 or 1	0

14.2.2 SPI1 register description

SPI1 status register (SPI1_STAT):

Bit	Name	Access	Description	Reset value
[7:5]	Reserved	RO	Reserved	000b
4	bS1_IF_BYTE	RW	Data byte transmission done interrupt flag bit 1: One byte transmission is done. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset, or reset by FIFO valid operation when bS1_AUTO_IF=1.	0
3	S1_FREE	RO	SPI1 free flag bit 1: No SPI shift at present, usually it is in free period between data bytes.	1
[2:0]	Reserved	RO	Reserved	000b

SPI1 receive/transmit data register (SPI1_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI1_DATA	RW	SPI data shift register actually. Read operation is used to receive data, and write operation is used to transmit data. Valid read/write operation can start one SPI transmission.	xxh

SPI1 control register (SPI1_CTRL):

Bit	Name	Access	Description	Reset value
7	bS1_MISO_OE	RW	MISO1 output enable bit of SPI1 1: Enabled. 0: Disabled.	0
6	Reserved	RO	Reserved	0
5	bS1_SCK_OE	RW	SCK1 output enable bit of SPI1 1: SCK1 output enabled. If bS1_2_WIRE=0, MOSI1 output is enabled at the same time. 0: Disabled.	0
4	bS1_DATA_DIR	RW	SPI1 data direction control bit. 0: Output. Only write SPI1_DATA operation is regarded as valid, and start one SPI transmission. 1: Input. Write/read SPI1_DATA operation is regarded as valid, and start one SPI transmission.	0
3	bS1_MST_CLK	RW	SPI1 clock mode control bit 0: Mode 0. SCK1 is at low level by default when idle. 1: Mode 3. SCK1 is at high level by default.	0
2	bS1_2_WIRE	RW	2-wire half-duplex mode enable bit of SPI1 0: 3-wire full-duplex mode (SCK1, MOSI1 and MISO1). 1: 2-wire half-duplex mode (SCK1, MISO1).	0
1	bS1_CLR_ALL	RW	1: Empty SPI1 interrupt flag and FIFO. Cleared by software.	1
0	bS1_AUTO_IF	RW	Byte receive done interrupt flag auto reset enable bit through SPI1_DATA valid operation. 1: Automatically reset the byte receive done interrupt flag (bS1_IF_BYTE) during valid read/write operation of SPI1_DATA.	0

SPI1 clock setting register (SPI1_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI1_CK_SE	RW	Set SPI1 clock frequency division factor.	20h

14.3 SPI transfer format

SPI host mode supports two transfer formats (mode0 and mode3). You can select it by setting the bSn_MST_CLK bit in SPI control register (SPIn_CTRL). CH555 always samples MISO data on the rising edge of CLK. The data transfer format is shown in the figure below.

Mode 0: bSn_MST_CLK = 0

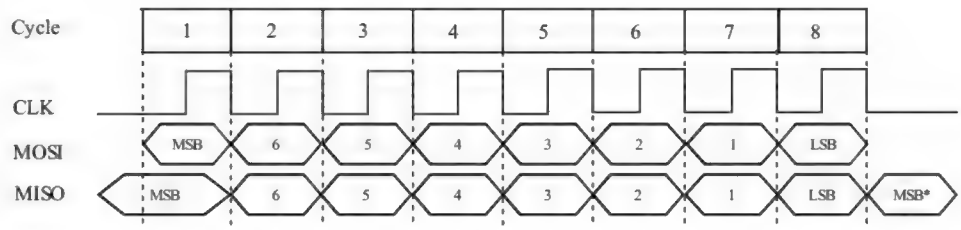


Figure 14.3.1 SPI mode 0 timing diagram

Mode 3: bSn_MST_CLK = 1

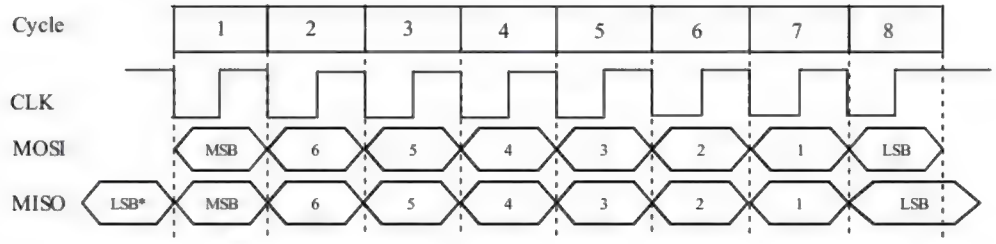


Figure 14.3.2 SPI mode 3 timing diagram

14.4 SPI configuration

14.4.1 Master mode

In SPI master mode, SCK pin outputs serial clock, and Chip Select output pin can be specified as any I/O pin.

SPI0 configuration procedure:

(1). Set the SPI clock setting register (SPI0_CK_SE), to configure SPI clock frequency.

(2). Set the bS0_MODE_SLV bit in the SPI setting register (SPI0_SETUP) to 0, to select master mode.

(3). Set the bS0_MST_CLK bit in the SPI control register (SPI0_CTRL), to select mode0 or mode3 as required.

(4). Set bS0_SCK_OE and bS0_MOSI_OE in the SPI control register (SPI0_CTRL) to 1, and set bS0_MISO_OE to 0, to set the P1 port direction bSCK and bMOSI as output, bMISO as input, and Chip Select pin as output.

Data transmission procedure:

(1). Write to the SPI0_DATA register, write the data to be transmitted to FIFO to automatically start one SPI transmission.

(2). Wait for S0_FREE to be 1, it indicates that the transmission is completed and the next byte can be sent.

Data reception procedure:

(1). Write to the SPI0_DATA register, write any data to FIFO, e.g. 0FFh, to start one SPI transmission.

(2). Wait for S0_FREE to be 1, it indicates that the reception is completed and SPI0_DATA can be read to obtain the received data.

(3). If bS0_DATA_DIR was set to 1 previously, the above read operation will also start the next SPI transmission, otherwise it will not start.

14.4.2 Slave mode

In slave mode, SCK pin is used to receive the serial clock of the connected SPI host.

(1). Set the bS0_MODE_SLV bit in the SPI0 setting register (SPI0_SETUP) to 1, to select slave mode.

(2). Set bS0_SCK_OE and bS0_MOSI_OE in the SPI0 control register (SPI0_CTRL) to 0, and set bS0_MISO_OE to 1, to set the P1 port direction bSCK, bMOSI and bMISO as well as chip select pin as input. When SCS is valid (low level), MISO will automatically enable output. At the same time, it is recommended to set MISO pin in high impedance input mode (P1_MOD_OC[6]=0, P1_DIR_PU[6]=0), so that MISO will not output during invalid chip select, that is convenient for sharing SPI bus.

(3). Optionally, set the preset data register (SPI0_S_PRE) in SPI slave mode, to be automatically loaded into the buffer for the first time after chip select for external output. After 8 serial clocks, that is, the first byte of data transmission exchange is completed, CH555 obtains the first byte of data (possibly command code) sent by the external SPI host, and the external SPI host obtains the preset data (possibly the status value) in SPI0_S_PRE through exchange. The bit7 in the SPI0_S_PRE register is automatically loaded into MISO pin during period of low-level SCK after SPI chip select is valid. In SPI mode 0, if bit 7 in SPI0_S_PRE is preset by CH555, the external SPI host will obtain the preset value of bit 7 in SPI0_S_PRE by inquiring MISO pin when SPI chip select is valid but there is no data transmission, thereby the value of bit 7 in SPI0_S_PRE can be obtained only by making SPI chip select effective.

Data transmission procedure:
Inquire S0_IF_BYTE or wait for interrupt, and after each SPI data byte transmission, write SPI0_DATA register, write the data to be sent to FIFO. Or wait for S0_FREE to be changed from 0 to 1, and the next byte can be sent.

Data reception procedure:
Inquire S0_IF_BYTE or wait for interrupt, and after each SPI data byte transmission, read SPI0_DATA register, obtain the data received from FIFO. Inquire S0_R_FIFO to know whether there are remaining bytes in FIFO.

15. Analog-to-digital converter (ADC)

15.1 Introduction to ADC and CMP

CH555 provides a 12-bit analog-to-digital converter, including analog-to-digital converter (ADC) and voltage comparator (CMP) module.

This ADC, with 14 external analog signal input channels and 2 internal input channels (reference voltage), can realize time-sharing acquisition, and supports analog input voltage from 0 to VDD.

There are two input options for the positive phase input of CMP: when bCMP_PIN=1, select to connect to the ADC analog input channel via resistor partial voltage. When bCMP_PIN=0, select to input VDD power through resistor partial voltage. The reference voltage of the inverted input is selected by MASK_CMP_VREF, generally the CMP is mainly used for supply voltage monitor and DC-DC control. Refer to Section 7.2.

15.2 ADC register

Table 15.2.1 ADC related registers

Name	Address	Description	Reset value
ADC_CTRL	F3h	ADC control and status register	xxh
ADC_DAT_H	F5h	ADC result data high byte (read only)	0xh
ADC_DAT_L	F4h	ADC result data low byte (read only)	xxh
ADC_DAT	F4h	ADC_DAT_L and ADC_DAT_H constitute a 16-bit SFR	0xxxh
ADC_CHAN	F6h	ADC analog signal channel selection register	00h

ADC control and status register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Reserved	00b
5	bADC_IF	RW	ADC conversion completed interrupt flag 1: One ADC conversion is completed. Cleared by writing 1, or cleared when writing ADC_CHAN data.	0
4	bADC_START	RW	ADC start control bit. Set 1 to start an ADC conversion, the bit is cleared automatically after the ADC conversion is completed.	0
3	bADC_EN	RW	Power control bit of ADC module 0: Turn off the power supply of the ADC module and enter the sleep state. 1: ON.	0
2	Reserved	RO	Reserved	0
1	bADC_CLK1	RW	ADC reference clock frequency selection high bit	0
0	bADC_CLK0	RW	ADC reference clock frequency selection low bit	0

Table 15.2.2 ADC reference clock frequency selection table

bADC_CLK1	bADC_CLK0	ADC reference clock frequency	Time required to complete an ADC	Applicable scope
0	0	750KHz	512 Fosc cycles	Rs<=20KΩ or Cs>=0.08uF
0	1	1.5MHz	256 Fosc cycles	Rs<=10KΩ or Cs>=0.08uF
1	0	3MHz	128 Fosc cycles	VDD>=3V and (Rs<=5KΩ or Cs>=0.08uF)
1	1	6MHz	64 Fosc cycles	VDD>=4.5V and (Rs<=2KΩ or Cs>=0.08uF)

Notes: VDD refers to supply voltage, Cs refers to capacitance in parallel with signal source, Rs refers to internal resistance in serial with signal source (the sampling time is only 4 reference clocks)

ADC analog signal channel selection register (ADC_CHAN):

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0000b
[3:0]	MASK_ADC_CHAN	RW	When bADC_EN=1, select the signal source of the analog signal channel; When bADC_EN=0, the analog signal channel will be closed	0000b

Table 15.2.1 Positive phase input of CMP and ADC input external signal channel selection table

bADC_EN	ADC_CHAN	Select the signal source of the analog signal channel
0	xxxxb	Disconnect internal and external signal channels (AIN0 ~ AIN13), suspended
1	0000b	Connect to external signal: AIN0 (P1.0)
1	0001b	Connect to external signal: AIN1 (P1.1)
1	0010b	Connect to external signal: AIN2 (P1.2)
1	0011b	Connect to external signal: AIN3 (P1.3)

1	0100b	Connect to external signal: AIN4 (P1.4)
1	0101b	Connect to external signal: AIN5 (P1.5)
1	0110b	Connect to external signal: AIN6 (P1.6)
1	0111b	Connect to external signal: AIN7 (P1.7)
1	1000b	Connect to external signal: AIN8 (P0.0)
1	1001b	Connect to external signal: AIN9 (P0.1)
1	1010b	Connect to external signal: AIN10 (P0.2)
1	1011b	Connect to external signal: AIN11 (P0.3)
1	1100b	Connect to external signal: AIN12 (P0.4)
1	1101b	Connect to external signal: AIN13 (P0.5)
1	1110b	Connect to internal reference voltage: V33 voltage
1	1111b	Connect to internal reference voltage: 1.8V voltage VREF18 (there may be noise)

ADC data register (ADC_DAT):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DAT_H	RO	High byte of ADC sampling result data	0xh
[7:0]	ADC_DAT_L	RO	Low byte of ADC sampling result data	xxh

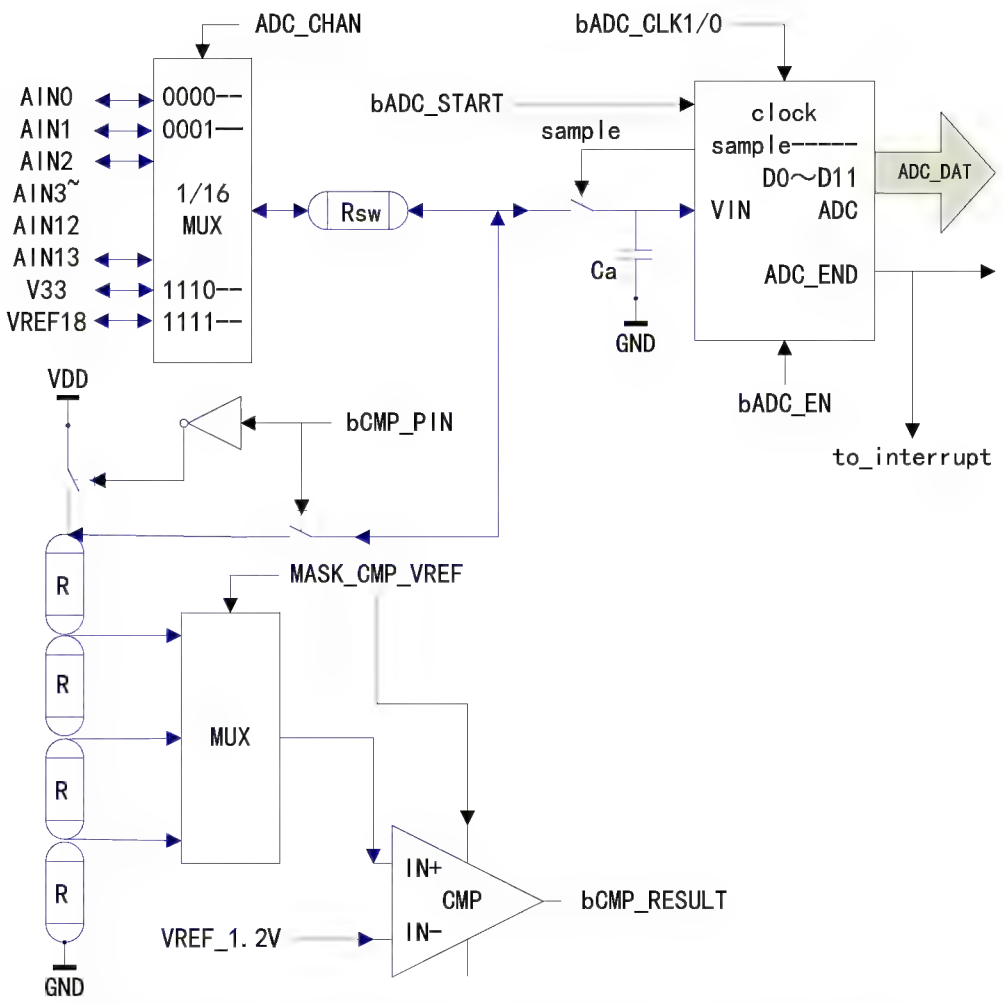


Figure 15.2.1 ADC structure diagram (Blue line represents analog signal)

15.3 ADC function

ADC sampling mode configuration procedure:

(1). Set the bADC_EN bit in ADC_CTRL register as 1, to enable ADC module, and set bADC_CLK0/1 to select frequency.

(2). Set ADC_CHAN register, to select external or internal signal channel.

(3). Optional, reset the bADC_IF interrupt flag. Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(4). Set bADC_START in ADC_CTRL register, to start an ADC conversion.

(5). Wait for bADC_START to be changed to 0, or bADC_IF to be set to 1 (if cleared before), it indicates that ADC conversion is completed, the result data can be read through ADC_DAT. This data is the value of the input voltage relative to 4095 equal parts of the VDD supply voltage. For example, if the result data is 475, it indicates that the input voltage is approximate to 475/4095 of VDD voltage. If VDD supply voltage is also uncertain, another certain reference voltage value can be measured, and calculate the measured input voltage value and VDD supply voltage value proportionally.

(6). If bADC_START is set again, start the next ADC conversion.

(7). If the ADC reference clock frequency is high and that results in a short sampling time, or high internal resistance in serial with signal source or low supply voltage results in a large Rsw internal resistance, then it is possible that Ca could not sample enough signal voltage and affect the ADC result. The solution is to discard the first ADC data, immediately start the second ADC and use its ADC result data, namely sampling twice.

(7). In case of high accuracy requirement, it is recommended to calibrate before use and eliminate the inherent deviation with software.

For the above selected external analog signal channel, the corresponding GPIO pin must be set in either high-impedance input mode or open-drain output mode and in output 1 state (equivalent to high-impedance input), Pn_DIR_PU[x]=0, and turn off the pull-up resistor and pull-down resistor.

16. USB Controller

16.1 Introduction

CH555 integrates a USB composite device controller, which is composed of a USB device-hub (USBHB) to support 3 HID function sub-devices (USBD0, USBD1 and USBD2) at the same time.

Main features of CH555 USB controller:

(1). Support USB control transfer, bulk transfer, interrupt transfer, synchronous/simultaneous transfer;

(2). Support data packet of up to 64 bytes, built-in FIFO, support interrupt and DMA;

(3). Support USB 2.0 full-speed (12Mbps) traffic;

(4). The composite device controller is composed of a built-in device-hub and 3 independent functional sub-devices;

(5). Optionally, turn off the composite device and only enable USBD0 device.

16.2 Function

The built-in USBHB provides 3 endpoints: Endpoint 0 is the default endpoint and supports control transfer, the transmission and reception share a 64-byte data buffer. Endpoint 1 is the transmission endpoint IN, with a separate 64-byte data buffer, supports bulk transfer, interrupt transfer and simultaneous/synchronous

transfer. Endpoint 4 is the optional reception endpoint OUT, using the last 32 bytes of 64-byte data buffer of endpoint 0, supports bulk transfer, interrupt transfer and simultaneous/synchronous transfer.

0# function sub-device USBD0 provides 7 endpoints: Endpoint 0 is the default endpoint and supports control transmission, the transmission and reception share a 64-byte data buffer. Endpoint 1, endpoint 2, and endpoint 3 can be independently configured as the transmission endpoint IN or reception endpoint OUT, each with a separate 64-byte data buffer, support bulk transfer, interrupt transfer and simultaneous/synchronous transfer. Endpoint 4 is the optional reception endpoint OUT, using the last 32 bytes of 64-byte data buffer of endpoint 0, supports bulk transmission, interrupt transmission and real-time/synchronous transmission. Endpoint 5 and endpoint 6 are the optional independent sending endpoints IN, using the last 32 bytes of the 64-byte data buffer of endpoint 1 and endpoint 2 respectively, support bulk transfer, interrupt transfer and simultaneous/synchronous transfer.

Since the three functional sub-devices have the same structure, only USBD0 is selected for description here.

Each endpoint has a control register (D0_EPnRES) and a transmission length register (D0_EPnT_L), used to set the synchronization trigger bit of endpoint, the response to OUT transactions or IN transactions and the length of data to be sent.

As the necessary USB bus pull-up resistor of USB device, it can be set whether to be enabled by the software at any time. When bUX_DP_PU_EN in USB_CTRL is set to 1, CH555 will connect the pull-up resistor internally to DP pin and enable the USB composite device function.

When USB is connected to the computer, device-hub enumeration will be conducted at first, and then each functional sub-device will be enumerated in turn according to the connection state of the downstream port of the hub. Finally, the USB data communication can be realized between the computer and each functional sub-device by time sharing.

When a USB bus reset, bus suspended or wake-up event is detected, or when the USB successfully processes data reception/transmission, the USB protocol processor will set corresponding interrupt flag and generate interrupt request. The application program can directly query or analyze USB_IF, D0_STATUS or HB_STATUS in the USB interrupt service program, and can directly clear the corresponding interrupt flag in USB_IF after processing the data transmission interrupt transaction. Each functional sub-device only needs to deal with USB data transmission interrupt bUX_IF_D0_TRANS, USBHB needs to deal with USB data transmission interrupt bUX_IF_HB_TRANS and bus reset interrupt bUX_IF_BUS_RST, bus suspended or wake-up interrupt bUX_IF_SUSPEND, FIFO overflow interrupt bUX_IF_FIFO_OV and other public transactions.

All data buffers of USB have fixed addresses, and the start address of data buffers of endpoint 0 is calculated as follows:

```
#define  pDi_EP0_BUF(i)  ((PUINT8X)(i*0x100+0x1000+UX_EP0_ADDR))
```

i refers to the serial number of sub-device from 0 to 3, and 3 represents device-hub here.

After the 64-byte buffer of endpoint 0 (optional endpoint 4 occupies the last 32 bytes), every 64 bytes are the respective 64-byte buffers of endpoint 1 (optional endpoint 5 occupies the last 32 bytes), 64-byte buffers of endpoint 2(optional endpoint 6 occupies the last 32 bytes), and 64-byte buffers of endpoint 3.

For example:
The buffer start address of USBD1 endpoint 0 is (1*0x100+0x1000+UX_EP0_ADDR)=0x1100;

The buffer start address of USBD1 endpoint 5 is 0x1100+64+32=0x1160.

16.3 Register

Table 16.3.1 USB global and USBHB related registers

Name	Address	Description	Reset value
USB_CTRL	223Ch	USB control register	0000 011xb
USB_IE	223Bh	USB interrupt enable register	0010 0000b
USB_IF	223Dh	USB interrupt flag register	0000 x000b
HB_STATUS	223Fh	USBHB status register	0001 1xxxb
HB_RX_LEN	223Eh	USBHB reception length register (read-only)	0xxx xxxxb
HB_ADDR	2237h	USBHB device address register	0000 0000b
HB_EP0RES	2230h	USBHB endpoint 0 control register	0000 0000b
HB_EP0T_L	2238h	USBHB endpoint 0 transmission length register	0xxx xxxxb
HB_EP1RES	2231h	USBHB endpoint 1 control register	0000 0000b
HB_EP1T_L	2239h	USBHB endpoint 1 transmission length register	00xx xxxxb
HB_EP4RES	2234h	USBHB endpoint 4 control register	0000 0000b

Table 16.3.2 USBD0 related registers

Name	Address	Description	Reset value
D0_EP_MOD	220Ch	USBD0 endpoint mode control register	0000 0000b
D0_STATUS	220Fh	USBD0 status register	0001 1xxxb
D0_RX_LEN	220Eh	USBD0 reception length register (read-only)	0xxx xxxxb
D0_ADDR	2207h	USBD0 device address register	0000 0000b
D0_EP0RES	2200h	USBD0 endpoint 0 control register	0000 0000b
D0_EP0T_L	2208h	USBD0 endpoint 0 transmission length register	0xxx xxxxb
D0_EP1RES	2201h	USBD0 endpoint 1 control register	0000 0000b
D0_EP1T_L	2209h	USBD0 endpoint 1 transmission length register	0xxx xxxxb
D0_EP2RES	2202h	USBD0 endpoint 2 control register	0000 0000b
D0_EP2T_L	220Ah	USBD0 endpoint 2 transmission length register	0xxx xxxxb
D0_EP3RES	2203h	USBD0 endpoint 3 control register	0000 0000b
D0_EP3T_L	220Bh	USBD0 endpoint 3 transmission length register	0xxx xxxxb
D0_EP4RES	2204h	USBD0 endpoint 4 control register	0000 0000b
D0_EP5RES	2205h	USBD0 endpoint 5 control register	0000 0000b
D0_EP5T_L	220Dh	USBD0 endpoint 5 transmission length register	00xx xxxxb
D0_EP6RES	2206h	USBD0 endpoint 6 control register	0000 0000b
D0_EP6T_L	220Eh	USBD0 endpoint 6 transmission length register	00xx xxxxb

Since the three functional sub-devices have the same structure, refer to the above-mentioned USBD0 description for USBD1 and USBD2 related registers.

USB control register (USB_CTRL)

Bit	Name	Access	Description	Reset value
7	bUX_DP_PU_EN	RW	USB device enable and DP pin internal pull-up resistor control bit 1: USB device transfer enabled and the internal	0

			1.5K pull-up resistor enabled.	
6	bUX_DM_PU_EN	RW	USB device enable and DM pin internal pull-up resistor control bit. 1: USB device transfer enabled and the internal 1.5K pull-up resistor enabled.	0
5	Reserved	RO	Reserved	0
4	bUX_HUB_EP4_EN	RW	USB device enable and USBHB endpoint4 enable bit. 1: USB device transfer enabled and endpoint4 enabled. 0: Endpoint4 disabled.	0
3	bUX_INT_BUSY	RW	Auto-pause enable bit before USB transfer completed interrupt flag is not cleared. 1: It automatically pauses and responds to busy NAK before interrupt flag bUX_IF_??_TRANS is not cleared. 0: Not pause	0
2	bUX_RESET_SIE	RW	USB protocol processor software reset control bit. 1: Forcefully reset the USB protocol processor, requires software to clear.	1
1	bUX_CLR_ALL	RW	1: Empty USB interrupt flag and FIFO, requires software to clear.	1
0	bUXS_BUS_RESET	RO	USB bus reset status bit. 0: No bus reset at present. 1: Bus reset is in progress	x

The USB device control combination consists of bUX_DP_PU_EN, bUX_DM_PU_EN and bUX_HUB_EP4_EN:

bUX_DP_PU_EN	bUX_DM_PU_EN	bUX_HUB_EP4_EN	USB device control description
0	0	0	Disable USB composite device function and turn off the internal pull-up resistor
0	0	1	Enable USB composite device, turn off the internal pull-up resistor, require an external pull-up resistor
1	0	0	Enable USB composite device, turn on DP internal 1.5KΩ pull-up resistor
0	1	0	Enable USB composite device, turn on DM internal 1.5KΩ pull-up resistor

USB interrupt enable register (USB_IE):

Bit	Name	Access	Description	Reset value
7	bUX_IE_SOF	RW	1: Receive SOF packet interrupt enabled; 0: Disabled	0
6	bUX_IE_NAK	RW	1: Rceive NAK interrupt enabled 0: Disabled	0

5	bUX_SIE_FREE	RO	Free status bit of USB protocol processor 0: Busy, USB transfer is in progress; 1: Idle	1
4	bUX_IE_FIFO_OV	RW	1: FIFO overflow interrupt enabled; 0: Disabled	0
3	bUX_R_FIFO_RDY	RO	USB receive FIFO data ready status bit. 0: Receive FIFO empty; 1: Receive FIFO not empty (with data).	0
2	bUX_IE_SUSPEND	RW	1: USB bus suspend/wakeup event interrupt enabled; 0: Disabled.	0
1	bUX_IE_TRANSFER	RW	1: USB transfer completed interrupt enabled; 0: Disabled.	0
0	bUX_IE_BUS_RST	RW	1: USB bus reset event interrupt enabled; 0: Disabled.	0

USB interrupt flag register (USB_IF):

Bit	Name	Access	Description	Reset value
7	bUX_IF_D2_TRANS	RW	USBD2 sub-device data transfer completed interrupt flag bit. 1: Interrupt, triggered by USBD2 transfer completed; 0: No interrupt. Write to D2_STATUS to clear.	0
6	bUX_IF_D1_TRANS	RW	USBD1 sub-device data transfer completed interrupt flag bit. 1: Interrupt, triggered by USBD1 transfer completed; 0: No interrupt. Write to D1_STATUS to clear.	0
5	bUX_IF_D0_TRANS	RW	USBD0 sub-device data transfer completed interrupt flag bit. 1: Interrupt, triggered by USBD0 transfer completed; 0: No interrupt. Write to D0_STATUS to clear.	0
4	bUX_IF_FIFO_OV	RW	USB FIFO overflow interrupt flag bit. 1: FIFO overflow interrupt. 0: No interrupt. Write 1 to clear.	0
3	bUX_SUSPEND	RO	USB bus suspend status bit. 0: There is USB activity at present. 1: There has been no USB activity for some time, request to be suspended	0
2	bUX_IF_SUSPEND	RW	USB bus suspend/wakeup event interrupt flag bit. 1: Interrupt, triggered by suspend/wakeup event (refer to bUX_SUSPEND for judgment). 0: No interrupt. Write 1 to clear.	0
1	bUX_IF_HB_TRANS	RW	USBHB hub self-data transfer completed interrupt flag bit. 1: Interrupt, triggered by USBHB transfer completed. 0: No interrupt. Write to HB_STATUS to clear.	0

0	bUX_IF_BUS_RST	RW	USB bus reset event interrupt flag bit. 1: Interrupt, triggered by the bus reset event. 0: No interrupt. Write 1 to clear.	0

USBHB status register (HB_STATUS), USBD0 status register (D0_STATUS):

Bit	Name	Access	Description	Reset value
7	bUXS_IS_NAK	RO	1:NAK busy response is received during current transfer.	0
6	bUXS_TOG_OK	RO	Current USB transfer DATA0/1 synchronization flag match state. 1: Synchronous; 0: Asynchronous.	0
5	bUXS_SETUP_ACT	RO	1: 8-byte SETUP request packet has been successfully received. SETUP token does not affect bUXS_TOG_OK and MASK_UXS_TOKEN, MASK_UXS_ENDP and X*_RX_LEN	0
[4:3]	MASK_UXS_TOKEN	RO	Token PID identification of the current USB transmission transaction: 00: OUT packet; 01: SOFpacket; 10: IN packet; 11: idle	11
[2:0]	MASK_UXS_ENDP	RO	Endpoint No. of the current USB transfer transaction: 000: Endpoint 0; ... ; 111: Endpoint 7	xxxb

When MASK_UXS_TOKEN is not idle, and bUXS_SETUP_ACT is also 1, it indicates that SETUP is right behind OUT or IN, and required to process the former first, clear bUX_IF_*_TRANS once after the former is processed to make the former enter the idle state, and then process the latter, and finally clear bUX_IF_*_TRANS again.

USBHB reception length register (HB_RX_LEN), USBD0 reception length register (D0_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	HB_RX_LEN D0_RX_LEN	RO	Number of data bytes received by the current USB endpoint, For USBD0/USBD1/USBD2, when bUX_EP6I_EN=1 and bUX_IE_TRANSFER=0, this register cannot be read	xxh

USBHB device address register (HB_ADDR), USBD0 device address register (D0_ADDR):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
[6:0]	MASK_USB_ADDR	RW	Address of USB device	00h

USBHB endpoint 0 control register (HB_EP0RES), USBD0 endpoint 0 control register (D0_EP0RES):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	Synchronization trigger bit expected by the	0

			receiver of USB endpoint 0 (handle SETUP/OUT). 0: Expect DATA0. 1: Expect DATA1	
6	bUEP_T_TOG	RW	Synchronization trigger bit prepared by the transmitter of USB endpoint 0 (handle IN). 0: Transmit DATA0. 1: Transmit DATA1	0
[5:4]	Reserved	RO	Reserved	00b
[3:2]	MASK_UEP_R_RES	RW	Set the response way of the receiver of endpoint 0 to SETUP/OUT transactions: 00: Reply ACK or ready; 01: Reserved/disabled; 10: Reply NAK or busy; 11: Reply STALL or error	00b
[1:0]	MASK_UEP_T_RES	RW	Set the response way of the transmitter of endpoint 0 to IN transaction: 00: Reply DATA0/DATA1 or data ready and expected ACK; 01: Reserved/disabled; 10: Reply NAK or busy; 11: Reply STALL or error	00b

USBHB endpoint n control register (HB_EPnRES), USBD0 endpoint n control register (D0_EPnRES) (n=1~6):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUEP_X_TOG	RW	Synchronization trigger bit expected by the receiver of USB endpoint n (handle SETUP/OUT), or the synchronization trigger bit prepared by the transmitter (handle IN). 0: DATA0. 1: DATA1.	0
5	Reserved	RO	Reserved	0
4	bUEP_X_AUTO_TOG	RW	Synchronization trigger bit auto toggle enable bit 1: Auto toggle the corresponding synchronization trigger bit after successful reception or transmission. 0: Not auto toggle, but manual switch is allowed	0
[3:2]	Reserved	RO	Reserved	00b
[1:0]	MASK_UEP_X_RES	RW	Set the response way of the receiver of USB endpoint n to SETUP/OUT services or the response way of the transmitter to IN services: 00: Receiver reply ACK or ready, transmitter reply DATA0/DATA1 or data ready and expected ACK; 01: Receiver timeout/no response, transmitter	00b

			reply DATA0/DATA1 and expected no response, used to realize real-time/synchronous transmission; 10: Reply NAK or busy; 11: Reply STALL or error	

USBHB endpoint n transmission length register (HB_EPnT_L), USBD0 endpoint n transmission length register (D0_EPnT_L):

Bit	Name	Access	Description	Reset value
[7:0]	HB_EPnT_L	RW	Set the number of data bytes that USB endpoint n is ready to transmit	xxh
[7:0]	D0_EPnT_L	RW	Set the number of data bytes that USB endpoint n is ready to transmit	xxh
[7:0]	D0_EP6T_L	RW	Set the number of data bytes that USB endpoint 6 is ready to transmit, Read-back is only allowed when bUX_EP6I_EN=1 and bUX_IE_TRANSFER=0, otherwise it is write-only	xxh

USBD0 endpoint mode control register (D0_EP_MOD):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUX_EP6I_EN	RW	USBD0 endpoint 6 enable bit. 1: Endpoint 6 IN enabled, and the buffer is the last 32 bytes of endpoint 2. 0: Endpoint 6 disabled.	0
5	bUX_EP5I_EN	RO	USBD0 endpoint 5 enable bit. 1: Endpoint 5 IN enabled, and the buffer is the last 32 bytes of endpoint 1. 0: Endpoint 5 disabled.	0
4	bUX_EP4O_EN	RW	USBD0 endpoint 4 enable bit. 1: Endpoint 4 OUT enabled, and the buffer is the last 32 bytes of endpoint 0. 0: Endpoint 4 disabled.	0
3	bUX_EP3O_EN	RW	USBD0 endpoint 3 selected as OUT or IN. 0: Endpoint 3 IN enabled and OUT disabled. 1: OUT enabled and IN disabled.	0
2	bUX_EP2O_EN	RW	USBD0 endpoint 2 selected as OUT or IN. 0: Endpoint 2 IN enabled and OUT disabled. 1: OUT enabled and IN disabled.	0
1	bUX_EP1O_EN	RW	USBD0 endpoint 1 selected as OUT or IN. 0: Endpoint 1 IN enabled and OUT disabled. 1: OUT enabled and IN disabled.	0
0	bUX_DEV_EN	RW	USBD0 functional sub-device enable. 1: Sub-device enabled, and respond to USB	0

			communication. 0: Sub-device disabled.	

17. Inter-integrated circuit (I2C) interface

17.1 I2C introduction

CH555 provides I2C slave I2CS interface. The main features are as follows:

(1). I2C slave controller is mainly used to externally simulate EEPROM memory 24CXX chip;

(2). I2C slave controller supports continuous read as well as DMA and interrupt;

(3). I2C slave controller can preset local slave address, and support broadcast address;

(4). I2C interface pins are built with controllable pull-up resistor, and no external pull-up resistor is required for the medium and low speed applications.

17.2 I2C global register

Table 17.2.1 I2C global related registers

Name	Address	Description	Reset value
I2CX_INT	B3h	I2C and RGB LED interrupt request register	0000 0000b
I2CS_INT_ST	BBh	Mapping of I2CS slave status register I2CS_STAT	0000 1100b

I2C and RGB LED interrupt request register (I2CX_INT):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Reserved	00b
5	bI2CS_INT_ACT	RO	I2CS interrupt request state. 0: Idle, and there is no interrupt request. 1: I2CS is requesting interrupt	0
4	Reserved	RO	Reserved	0
[3:2]	Reserved	RO	Reserved	00b
1	bLED_INT_ACT	RO	RGB LED interrupt request state. 0: Idle, and there is no interrupt request. 1: RGB LED is requesting interrupt	0
0	Reserved	RO	Reserved	0

I2CS slave status register mapping (I2CS_INT_ST), I2CS slave status register (I2CS_STAT):

Bit	Name	Access	Description	Reset value
7	bI2CS_IF_STASTO	RW	Received START or STOP condition interrupt flag bit. 1: There is an interrupt. START or STOP is further determined according to MASK_I2CS_STAT. 0: There is no interrupt. Write 1 to reset	0
6	bI2CS_IF_BYTE	RW	A data byte transfer completed interrupt flag bit. 1: There is an interrupt, triggered after a byte is received/transmitted. 0: There is no interrupt. Write 1 to reset	0
5	bI2CS_IF_ADDR	RW	Received data unit address interrupt flag bit.	0

			1: There is an interrupt, triggered after the data address is received. 0: There is no interrupt. Write 1 to reset	
4	bI2CS_IF_DEV_A	RW	Received slave device address interrupt flag bit. 1: There is an interrupt, triggered after the slave address is received, no matter the address matches or not. 0: There is no interrupt. Write 1 to reset	0
[3:0]	MASK_I2CS_STAT	RO	I2CS slave current status: 0000: Idle, or is receiving slave address; 0001: Reply the received slave address; 0010: Is receiving data unit address; 0011: Reply the received data unit address; 0100: Is receiving data byte; 0101: Reply the received data byte; 0110: Is sending data byte; 0111: Is waiting and checking the reply after the data is sent; 1100: In STOP condition; XXXX: Unknown status	1100b

17.3 I2C slave register

Table 17.3.1 I2CS slave related registers

Name	Address	Description	Reset value
I2CS_CTRL	2232h	I2CS slave control register	0000 0x00b
I2CS_DEV_A	2233h	I2CS slave device address register	0000 0000b
I2CS_ADDR	2235h	I2CS slave data address register (read-only)	xxxx xxxxb
I2CS_DATA	2236h	I2CS slave data receive/transmit register	xxxx xxxxb
I2CS_STAT	223Ah	I2CS slave status register	0000 1100b
I2CS_DMA_L	2139h	I2CS slave buffer start address low byte	xxxx xxxxb
I2CS_DMA_H	2138h	I2CS slave buffer start address high byte	000x xxxxb

I2CS slave control register (I2CS_CTRL):

Bit	Name	Access	Description	Reset value
7	bI2CS_IE_TRAN	RW	I2CS transmit data interrupt enable bit. 1: The interrupt is triggered after one data byte is transmitted. 0: The interrupt is not triggered.	0
6	bI2CS_IE_RECV	RW	I2CS receive data interrupt enable bit. 1: The interrupt is triggered after one data byte is received. 0: The interrupt is not triggered	0
5	bI2CS_IE_ADDR	RW	I2CS receive data address interrupt enable bit. 1: The interrupt is triggered after the data address	0

			is received. 0: The interrupt is not triggered	
4	bI2CS_IE_DEV_A	RW	I2CS receive slave address interrupt enable bit. 1: The interrupt is triggered after the slave address is received. 0: The interrupt is not triggered. If the bit is 1, the broadcast address is enabled, otherwise broadcast address is not supported.	0
3	bI2CS_IE_STASTO	RW	I2CS receive START or STOP consition interrupt enable bit. 1: The interrupt is triggered after the START or STOP condition is received. 0: The interrupt is not triggered	0
2	bI2CS_SDA_IN	RO	Current SDA0 pin status after synchronization: 0: Low level; 1: High level	x
1	bI2CS_DMA_EN	RW	I2CS read data DMA enable. 1: DMA enabled, only support DMA to read data, when the data is read by the external I2C host, it is automatically obtained via DMA before being sent. 0: DMA disabled and the data can be exchanged by reading/writing I2CS_DATA	0
0	bI2CS_EN	RW	I2CS slave enable. 0: I2CS slave disabled and reset. 1: I2CS slave enabled.	0

I2CS slave device address register (I2CS_DEV_A):

Bit	Name	Access	Description	Reset value
[7:1]	MASK_I2CS_DEV_A	RW	I2CS slave device address value 0: Broadcast address Others: The assigned slave device addresses that need to be matched.	00h
0	bI2CS_DA_4BIT	RW	I2CS0 slave device address mode: 0: 7-bit slave address mode, I2CS_ADDR is actually 8 bits; 1: 4-bit slave address mode, only the higher 4 bits of the slave device address need to be matched other than the lower 3 bits which are stored in MASK_I2CS_AH. When DMA is reading data, the actual extension of I2CS_ADDR is 11 bits, whose higher 3 bits are from MASK_I2CS_AH	0

I2CS slave data address register (I2CS_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_ADDR	RO	Store the data unit address specified by the external I2C host, automatically increased after each byte during a sequential read/write operation	xxh

I2CS slave data receive/transmit register (I2CS_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_DATA	RW	I2CS slave data receive/transmit register includes the transmit register and the receive register that are physically separated. The data written into this register is transmitted for external I2C host to read, or it can be read by DMA instead. Reading this register returns the data in the receive buffer, usually the data recently written by the external I2C host	xxh

I2CS slave status register (I2CS_STAT), refer to I2CS_INT_ST in Section 17.2.

I2CS slave buffer start address (I2CS_DMA_H, I2CS_DMA_L):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_DMA_H	RW	I2CS slave buffer start address high byte, only the lower 5 bits are valid. When bI2CS_DA_4BIT=0, the higher 3 bits are 0; when bI2CS_DA_4BIT=1, read the higher 3 bits and return to MASK_I2CS_AH	xxh
[7:5]	MASK_I2CS_AH	RO	When bI2CS_DA_4BIT=1, store the lower 3 bits of the received target slave device address, and the higher 3 bits as data unit address are used for DMA	xxxb
[7:0]	I2CS_DMA_L	RW	I2CS slave buffer start address low byte	xxh

When bI2CS_DA_4BIT=0, the current data DMA address = I2CS_DMA + I2CS_ADDR.

When bI2CS_DA_4BIT=1, the current data DMA address = I2CS_DMA + { MASK_I2CS_AH, I2CS_ADDR }.

18. RGB tri-color LED controller

18.1 RGB LED introduction

CH555 is built with RGB tri-color LED controller. The main features are as follows:

(1). 24-channel PWM (3*8) and 1/16 dynamic scanning, support 384 single-color LEDs or 128 groups of RGB tri-color LEDs;

(2). Optional 7-bit or 8-bit color PWM, the maximum 3* 8-bit color PWM supports 16777216 combined colors;

(3). Optional 6-bit or 7-bit or 8-bit brightness PWM, supports level-256 grayscale;

(4). Multistage adjustable blanking time, support color PWM repeated framing, and support 1/2 ~ 1/16 dynamic scanning.

(5). Dedicated DMA mode, support load the preset fixed data from Flash-ROM or the edited data from xRAM.

The following is the RGB LED drive structure of CH555, supports 384 single color LEDs, for reference only.

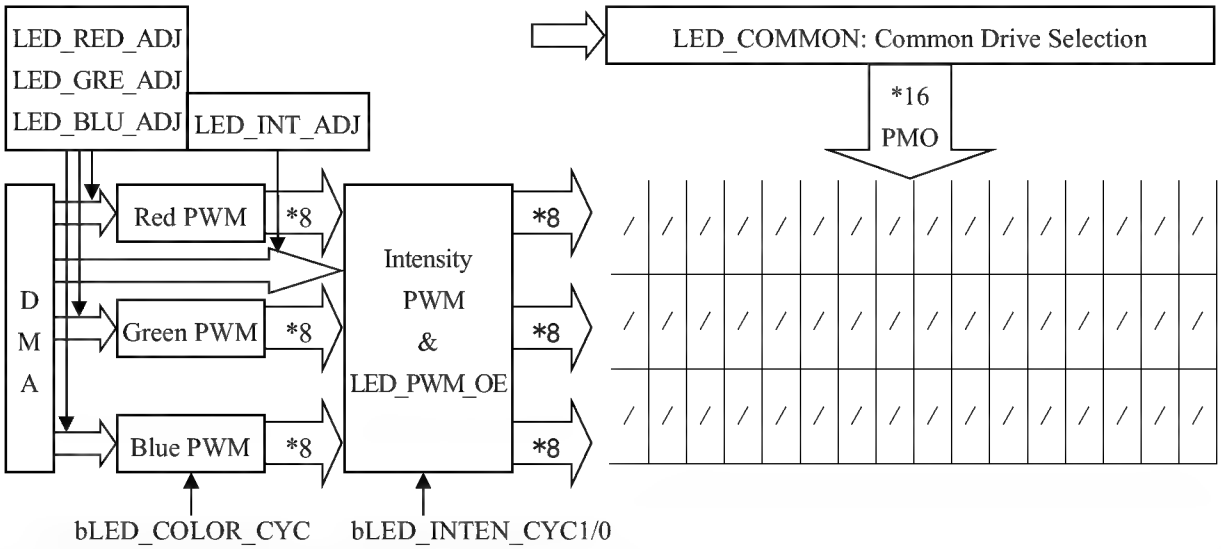


Table 18.1.1 RGB LED related registers

Name	Address	Description	Reset value
LED_CTRL	21D1h	RGB LED control register	0000 0000b
LED_CYCLE	21D2h	RGB LED cycle configuration register	0000 0000b
LED_FRAME	21D3h	RGB LED frame configuration register	0000 0000b
LED_PWM_OE	A7h	RGB LED drive PWM pin enable register	0000 0000b
LED_COMMON	A6h	RGB LED drive COMMON pin selection register	0000 0000b
LED_STATUS	F7h	RGB LED status register	0001 xxxxb
LED_DMA_H	C7h	RGB LED buffer area current address high byte	xxxx xxxxb
LED_DMA_L	C6h	RGB LED buffer area current address low byte	xxxx xxxxb
LED_DMA	C6h	LED_DMA_L and LED_DMA_H constitute a 16-bit SFR	xxxxh
LED_INT_ADJ	21D8h	RGB LED brightness adjustment register	0000 0000b
LED_RED_ADJ	21D9h	RGB LED red adjustment register	0000 0000b
LED_GRE_ADJ	21DAh	RGB LED green adjustment register	0000 0000b
LED_BLU_ADJ	21DBh	RGB LED blue adjustment register	0000 0000b
LED_FRA_STA	21DCh	RGB LED frame status register (read only)	0000 0000b
LED_COL_CNT	21DDh	RGB LED color counter register (read only)	0000 0000b

RGB LED control register (LED_CTRL):

Bit	Name	Access	Description	Reset value
7	bLED_IE_INHIB	RW	RGB LED frame end interrupt enable bit. 1: The interrupt is triggered at the end of a PWM. 0: The interrupt is not triggered	0
6	bLED_BLUE_EN	RW	Blue PWM pin group BLU0～BLU7 output enable. 0: Blue PWM output disabled. 1: Blue PWM enabled.	0

5	bLED_GREEN_EN	RW	Green PWM pin group GRE0~GRE7 output enable. 0: Green PWM output disabled. 1: Green PWM enabled	0
4	bLED_RED_EN	RW	Red PWM pin group RED0~RED7 output enable. 0: Red PWM output disabled. 1: Red PWM enabled.	0
3	bLED_COM_AHEAD	RW	RGB LED scanning driver pre-charging mode: 0: Normally start PMOS; 1: Start PMOS one clock in advance to allow its gate to charge	0
2	bLED_PWM_INHIB	RW	RGB LED automatic blanking mode: 0: Keep PWM output during scanning switch; 1: Automatic reset bLED_PWM0_OE at the end of the frame to automatically close PWM output during scanning switch;	0
1	Reserved	RO	Reserved	0
0	bLED_EN	RW	RGB LED enable. 0: RGB LED disabled and reset. 1: Start RGB LED clock.	0

RGB LED cycle configuration register (LED_CYCLE):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bLED_COLOR_CYC	RW	Select color PWM data width and PWM cycle: 0: 8 bits, 256 brightness PWM cycles; 1: 7 bits, 128 brightness PWM cycles	0
[5:4]	MASK_LED_INT_CYC	RW	Select brightness PWM data width and PWM cycle: 00: 8 bits, 256 reference clocks, used when COMMON is fewer; 01: 7 bits, 128 reference clocks, recommended; 10/11: 6 bits, 64 reference clocks, preferred.	00b
[3:2]	Reserved	RO	Reserved	00b
[1:0]	MASK_LED_CLK_FREQ	RW	Select RGB LED and brightness PWM reference clock: 00: Fsys; 01: Fsys/2; 10: Fsys/3; 11: Fsys/4	00b

RGB LED frame configuration register (LED_FRAME):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
[6:4]	MASK_LED_INH_TMR	RW	Select the scanning switch time with the brightness PWM cycle as the unit:	000b

			000~011: 1~4 brightness PWM cycles respectively: 100: 6 brightness PWM cycles; 101: 8 brightness PWM cycles; 110: 10 brightness PWM cycles; 111: 12 brightness PWM cycles	
3	Reserved	RO	Reserved	0
[2:0]	MASK_LED_PWM_REPT	RW	Select the number of color PWM repetitions in a PWM frame, 000~111: repeat 1~ 8 times respectively	000b

RGB LED drive PWM pin enable register (LED_PWM_OE):

Bit	Name	Access	Description	Reset value
7	bLED_PWM7_OE	RW	PWM7 pin group output enable. 0: PWM7 group output disabled. 1: PWM7 group output enabled.	0
6	bLED_PWM6_OE	RW	PWM6 pin group output enable. 0: PWM6 group output disabled. 1: PWM6 group output enabled.	0
5	bLED_PWM5_OE	RW	PWM5 pin group output enable. 0: PWM5 group output disabled. 1: PWM5 group output enabled.	0
4	bLED_PWM4_OE	RW	PWM4 pin group output enable. 0: PWM4 group output disabled. 1: PWM4 group output enabled	0
3	bLED_PWM3_OE	RW	PWM3 pin group output enable. 0: PWM3 group output disabled. 1: PWM3 group output enabled.	0
2	bLED_PWM2_OE	RW	PWM2 pin group output enable. 0: PWM2 group output disabled. 1: PWM2 group output enabled.	0
1	bLED_PWM1_OE	RW	PWM1 pin group output enable. 0: PWM1 group output disabled. 1: PWM1 group output enabled.	0
0	bLED_PWM0_OE	RW	PWM0 pin group and global PWM output enable. 0: PWM0 group and global PWM output disabled. 1: PWM0 group output enabled. When bLED_PWM_INHIB=1, this bit is automatically reset at the end of each PWM frame to realize automatic blanking during scanning switch	0

RGB LED drive COMMON pin selection register (LED_COMMON):

Bit	Name	Access	Description	Reset value
[7:0]	LED_COMMON	RW	Select the dynamically scanned COMMON pin, only	00h

			the lower 5 bits are valid: 01110: Select COM14, P7.0; 01111: Select COM15, P7.1; 10000~10111: Select COM16~COM23, P0.0~P0.7 respectively; 11000~11111: Select COM24~COM31, P3.0~P3.7 respectively	

RGB LED status register (LED_STATUS):

Bit	Name	Access	Description	Reset value
7	bLED_IF	RW	RGB LED frame end interrupt flag bit. 1: An end of frame has occurred. Write 1 to clear, or cleared when writing LED_COMMON (scanning switch)	0
6	bLED_IF_SET	WO	Write 1 to force bLED_IF to set 1, so as to enter the interrupt service program	0
5	Reserved	RO	Reserved	0
4	bLED_INHIB	RO	RGB LED frame state. If the bit is 1, it indicates idle or in scanning switch period that allows scanning switch and loading new data. If the bit is 0, it indicates in normal PWM drive period	1
[3:0]	MASK_LED_INTEN	RO	Higher 4 bits of brightness PWM counter	xxxx

RGB LED buffer current address (LED_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	LED_DMA_H	RW	RGB LED data buffer current address high byte	xxh
[7:0]	LED_DMA_L	RW	RGB LED data buffer current address low byte	xxh

RGB LED brightness adjustment register (LED_INT_ADJ), RGB LED red adjustment register (LED_RED_ADJ), RGB LED green adjustment register (LED_GRE_ADJ), RGB LED blue adjustment register (LED_BLU_ADJ):

Bit	Name	Access	Description	Reset value
[7:0]	LED_INT_ADJ	RW	RGB LED brightness adjustment value, -128~ 127, the highest bit represents symbol, The adjustment value is automatically added to the brightness PWM when the brightness data is loaded	00h
[7:0]	LED_RED_ADJ	RW	RGB LED red adjustment value, -128~127, the highest bit represents symbol, The adjustment value is automatically added to the red PWM when the red data is loaded	00h
[7:0]	LED_GRE_ADJ	RW	RGB LED green adjustment value, -128~127, the highest bit represents symbol, The adjustment value is automatically added to the green PWM when the green data is loaded	00h

[7:0]	LED_BLU_ADJ	RW	RGB LED blue adjustment value, -128~127, the highest bit represents symbol, The adjustment value is automatically added to the blue PWM when the blue data is loaded	00h

RGB LED frame status register (LED_FRA_STA):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
[6:4]	MASK_LED_REPEAT	RO	The repeated count value of the current color PWM within the PWM frame	000b
[3:0]	MASK_LED_INHIB	RO	The count value of the scanning switch time with the brightness PWM cycle as the unit at present	0000b

RGB LED color counter register (LED_COL_CNT):

Bit	Name	Access	Description	Reset value
[7:0]	LED_COL_CNT	RO	Color PWM counter	00h

19. Parameters

19.1 Absolute maximum ratings

Operating in critical ratings or exceeding the absolute maximum ratings may cause the chip to work abnormally or even be damaged)

Symbol	Parameter description		Min.	Max.	Unit
TA	Operating ambient temperature	Fsys<40MHz	-40	85	℃
		Test, Fsys=48MHz (bLDO_CORE_VOL=1 recommended)	-40	70	℃
TAROM	Ambient temperature for Flash-ROM/EEPROM erase/program operation (recommended)		-20	85	℃
TS	Ambient temperature during storage		-55	125	℃
VDD	Supply voltage (VDD connects to the power, GND to ground)		-0.4	7.0	V
V33	Internal USB supply voltage		-0.4	VDD+0.4	V
VIO	Voltage on the input/output pins		-0.4	VDD+0.4	V
VIOU	Voltage on USB pin DP/DM		-0.4	V33+0.4	V

19.2 Electrical characteristics (5V)

Test conditions: TA=25℃, VDD=5V, Fsys=12MHz

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD5	VDD pin supply voltage	V33 is only connected to an external capacitor	3.7	5	6.6	V
V33	Internal power regulator	TA=-15～65℃	3.23	3.3	3.57	V

	output voltage (Automatically short connected to VDD during sleep)	TA=-40～85℃	3.2	3.3	3.6	V
ICC32M5	Total supply current when Fsys=32MHz			6.2		mA
ICC12M5	Total supply current when Fsys=12MHz			3.4		mA
ICC750K5	Total supply current when Fsys=750KHz			1.5		mA
ISLP5	Total supply current after standby/normal sleep			1.1	1.4	mA
ISLP5L	bLDO_3V3_OFF=1, turn off LDO, Total supply current after power off/deep sleep			6	18	uA
IADC5	ADC module working current			200	600	uA
ICMP5	Voltage comparator module working current			70	100	uA
VIL5	Low level input voltage		0		1.2	V
VIH5	High level input voltage		2.6		VDD	V
VIHP6	P5/P6 pin high level input voltage		2.1		V33	
VOL5	Low level output voltage (20mA input current)				0.4	V
VOH5	High level output voltage (10mA output current)		VDD-0.4			V
VOLP6	P5/P6 pin low level output voltage (8mA input current)				0.4	V
VOHP6	P5/P6 pin high level output voltage (8mA output current)		V33-0.4			V
VOH5U	USB pin high level output voltage (8mA output current)		V33-0.4			V
IIN	Input current of input without pull-up resistor		-5	0	5	uA
IUP5	Input current of input with pull-up resistor other than P5/P6		35	70	110	uA
IUP5X	Input current of input with pull-up resistor from low to high		250	400	600	uA
IUP5I	Input current of input of I2C pin with pull-up resistor		330	660	1000	uA
Rsw5	ON resistance of the analog switch of ADC and other modules		500	700	1350	Ω
Vpot	Power on reset threshold		2.3	4.0	4.6	V

19.3 Electrical characteristics (3.3V)

Test conditions: TA=25℃, VDD=V33=3.3V, Fsys=12MHz

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD3	Supply voltage on VDD pin	V33 is shorted to VDD, turn on USB	3.0	3.3	3.6	V
		V33 is shorted to VDD, turn off USB	2.6	3.3	3.6	V

ICC32M3	Total supply current during operation at Fsys=32MHz		6.0		mA
ICC12M3	Total supply current during operation at Fsys=12MHz		3.3		mA
ICC750K3	Total supply current during operation at Fsys=750KHz		1.5		mA
ISLP3	Total supply current after standby/normal sleep		1.1	1.3	mA
ISLP3L	bLDO_3V3_OFF=1, turn off LDO, Total supply current after power off/deep sleep		3	13	uA
IADC3	ADC analog to digital conversion module working current		180	500	uA
ICMP3	Voltage comparator module working current		60	100	uA
VIL3	Low level input voltage	0		0.8	V
VIH3	High level input voltage	2.0		VDD	V
VOL3	Low level output voltage (12mA input current)			0.4	V
VOH3	High level output voltage (6mA output current)	VDD-0.4			V
VOLP6	P5/P6 pin low level output voltage (8mA input current)			0.4	V
VOHP6	P5/P6 pin high level output voltage (8mA output current)	V33-0.4			V
VOH3U	USB pin high level output voltage (8mA output current)	V33-0.4			V
IIN	Input current of input without pull-up resistor	-5	0	5	uA
IUP3	Input current of input with pull-up resistor	15	30	50	uA
IUP3X	Input current of input with pull-up resistor from low to high	100	170	260	uA
IUP3I	Input current of input of I2C pin with pull-up resistor	140	280	440	uA
Rsw3	On resistance of the analog switch of ADC and other modules	600	1000	2500	Ω
Vpot	Power-on reset threshold	2.3	2.7	3.0	V

19.4 Timing parameters

Test conditions: TA=25°C, VDD=5V or VDD=V33=3.3V, Fsys=12MHz

Symbol	Parameter description		Min.	Typ.	Max.	Unit
Fxt	External crystal frequency or XI input clock frequency		6	24	24	MHz
Fosc	Internal clock frequency after calibration when VDD>=3V	TA=-15～65°C	23.64	24	24.36	MHz
		TA=-40～85°C	23.5	24	24.5	MHz
Fosc3	When VDD<3V, the internal clock frequency after calibration		23.28	24	24.72	MHz
Fpll	Frequency after PLL		24	96	96	MHz

Fsys	System clock frequency (VDD>=3V)	0.1	12	48	MHz
	System clock frequency (VDD<3V)	0.1	12	24	MHz
Tpor	Power on reset delay	8	11	15	mS
Trst	Width of the input effective reset signal from the outside of RST#	2			uS
Trdl	Thermal reset delay	20	30	50	uS
Twdc	Calculation formula for watchdog overflow cycle/timing cycle	131072 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	Automatic USB suspension detection time in USB device mode	4	5	6	mS
Twaksb	Wake-up completion time after chip standby/normal sleep	0.5	0.8	3	uS
Twakdp	Wake-up completion time after chip power down/deep sleep	120	200	1000	uS

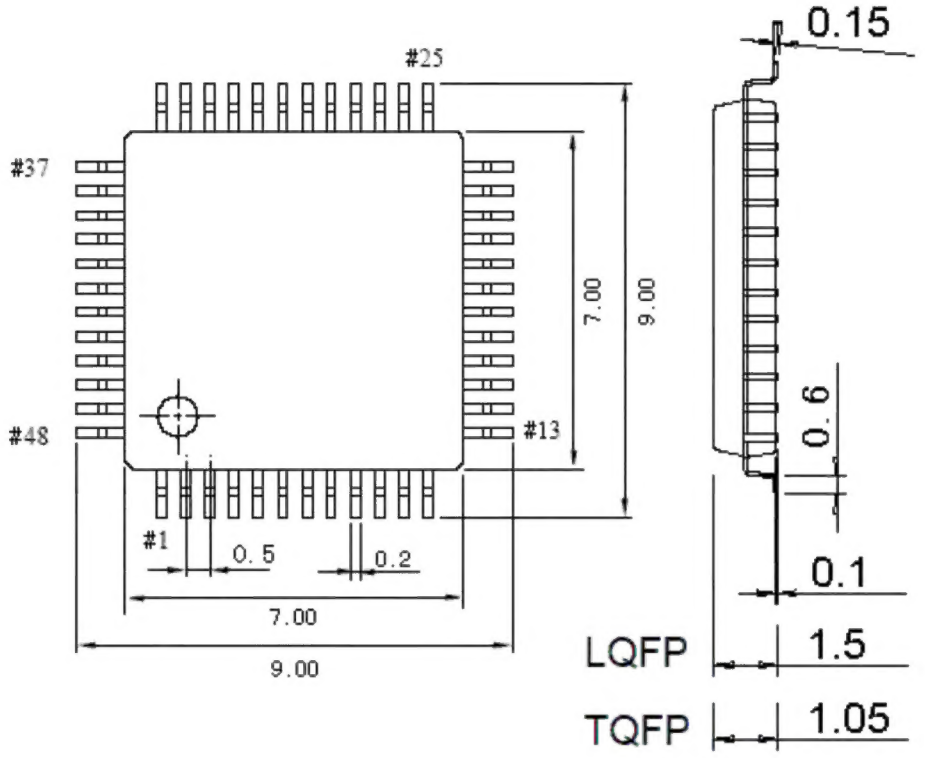
19.5 Other parameters

Test conditions: TA=25°C, VDD=4.5V～5.5V or VDD=V33=3.0V～3.6V

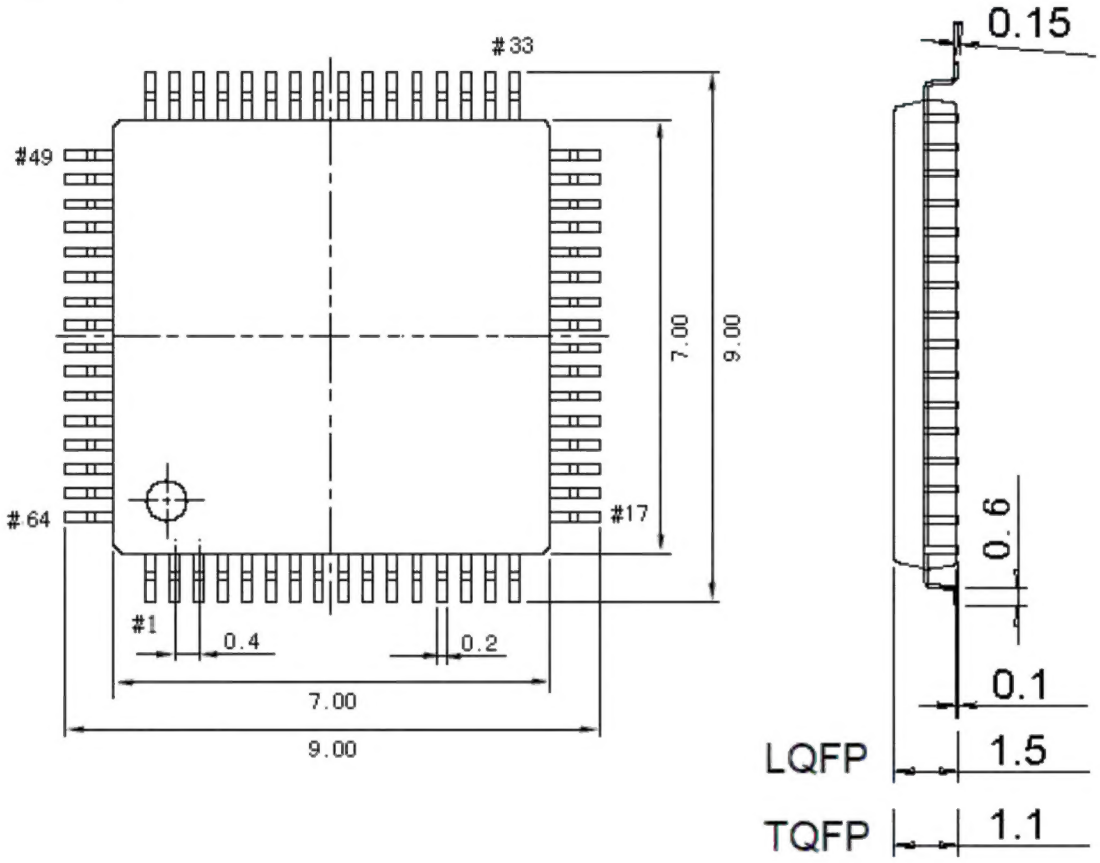
Symbol	Parameter description	Min.	Typ.	Max.	Unit
TERPG	Single erase/program operation time of Flash-ROM/EEPROM	2	5	8	mS
NEPCE	Erase/program cycle endurance	10K	Non-guaranteed 100K		times
TDR	Data hold capability of Flash-ROM/EEPROM	10			years
VESD	ESD voltage on I/O pins	4K	Non-guaranteed 8K		V

20. Package information

20.1 LQFP48-7*7



20.2 LQFP64-7*7



21. Revision history

Revision	Date	Description
V1.0	February 27, 2020	Official release
V1.1	March 22, 2021	Add description about switching to 7.5K pull-up resistor for USB sleep when 5V.
V1.2	July 5, 2021	Add introduction to CH555Q in LQFP64 package. Add description about P5 port and SPI1. Add note that it is stongly recommended to set bLDO_CORE_VOL=1 if system clock frequency is 48MHz. Add dedcription about selecting 8 bits for MASK_LED_INT_CYC only when COMMON is fewer
V1.3	December 9, 2021	Correct typos, exchange bI2CS_IE_TRAN and bI2CS_IE_RECV. Add note that USB pins are not needed to be connected with external resistors in series.
V1.4	January 5, 2022	Limit system clock frequency not to exceed 48 MHz. Optimize the description about clearing bit: Directly write 0 to clear, or write 1 to the corresponding bit in the register to clear.